2020

MotorComm YT8521SH YT8521SC Datasheet

INTEGRATED 10/100/1000 GIGABIT ETHERNET TRANSCEIVER

V1.02

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Revision History

Revision	Release Date	Summary
Draft	2019/09/07	
Draft 01	2019/09/12	Remove 1588 related information
Draft 02	2019/12/06	Add basic register
Draft 03	2019/12/20	Modify several description
Draft 04	2020/01/02	Modify Part Number
Draft 05	2020/01/22	Modify register description.
Draft 06	2020/02/17	1. Add mechanical information. 2. Modify several description
Draft 07	2020/02/25	Add several description.
Draft 08	2020/03/27	Modify several description.
V1.00	2020/03/30	Modfiy Fomat
V1.01	2020/03/31	Update Register Defalut Add block diagram Modify pin 43 type
V1.02	2020/03/31	Update Reg table

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1. General Description

The YT8521SH/YT8521SC is a highly integrated Ethernet transceiver that complies with 10Base-Te, 100Base-TX, and 1000Base-T IEEE 802.3 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT.5 UTP cable.

The YT8521SH/YT8521SC uses state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented in the YT8521SH/YT8521SC to provide robust transmission and reception capabilities at 10Mbps, 100Mbps, or 1000Mbps.

Data transfer between MAC and PHY is via the Reduced Gigabit Media Independent Interface (RGMII), or Serial Gigabit Media Independent Interface (SGMII) for 1000Base-T, 10Base-Te, and 100Base-TX. The YT8521SH/YT8521SC supports various RGMII signaling voltages, including 3.3, 2.5, and 1.8v.

The YT8521SH/YT8521SC also supports a SerDes interface that can be configured as SGMII, 1000Base-X, or 100Base-FX.

The YT8521SH/YT8521SC features the Extend-Range protocol on the MDI pins. Hyper-Range enables the device to auto-negotiate and link up with Extend-Range (YT multi-port PHY) compliant link partners in extended cable reach applications up to 400 meter @100Mbps, depending on cable type and individual cable parameters.

1.1. TARGET APPLICATIONS

- DTV (Digital TV)
- MAU (Media Access Unit)
- CNR (Communication and Network Riser)
- Game Console
- Printer and Office Machine
- DVD Player and Recorder
- Ethernet Hub
- Ethernet Switch
- PTP-featured Equipment with Ethernet Ports
- Base Stations and Controllers
- Routers, DSLAMs, PON Equipment
- Test and Measurement Systems
- Industrial and Factory Automation Equipment
- Multimedia synchronization and Real Time Networking
- Any embedded system with an Ethernet MAC that needs a UTP physical connection.

2. Feature

- 1000Base-T IEEE 802.3ab Compliant
- 100Base-TX IEEE 802.3u Compliant
- 10Base-Te IEEE 802.3 Compliant
- Support 4 pairs Extend Range
  - Cable reach up to 400 meter @100Mbps
- Supports RGMII/SGMI MAC interface
- Supports IEEE 802.3az-2010 (Energy Efficient Ethernet)
  - EEE Buffering
  - Incorporates EEE buffering for seamless support of legacy MACs
- Supports Synchronous Ethernet (Sync-E)
- Built-in Wake-on-LAN (WOL) over UTP/Fiber
- Supports Interrupt function over UTP/Fiber
- Supports Parallel Detection
- Crossover Detection & Auto-Correction
- Automatic polarity correction
- Baseline Wander Correction
- Supports 120m for CAT.5 cable in 1000Base-T
- Selectable 3.3/2.5/1.8v signaling for RGMII.
- Supports 25MHz external crystal or OSC
- Provides 125MHz clock source for MAC
- Provides 3 network status LEDs
- Supports Link Down power saving
- Built-in Switching Regulator and LDO
- Industrial grade manufacturing process

- Supports SERDES (SGMII/Fiber)
- Supports Fiber-to-UTP Media Convertor mode or SGMII-to-RGMII Bridge mode
- Supports UTP/Fiber Auto Detection
- Supports 18k bytes jumbo frame when 1000Base-T and 100Base-T, and 10k bytes when 10Base-T
- 48-pin QFN Green Package

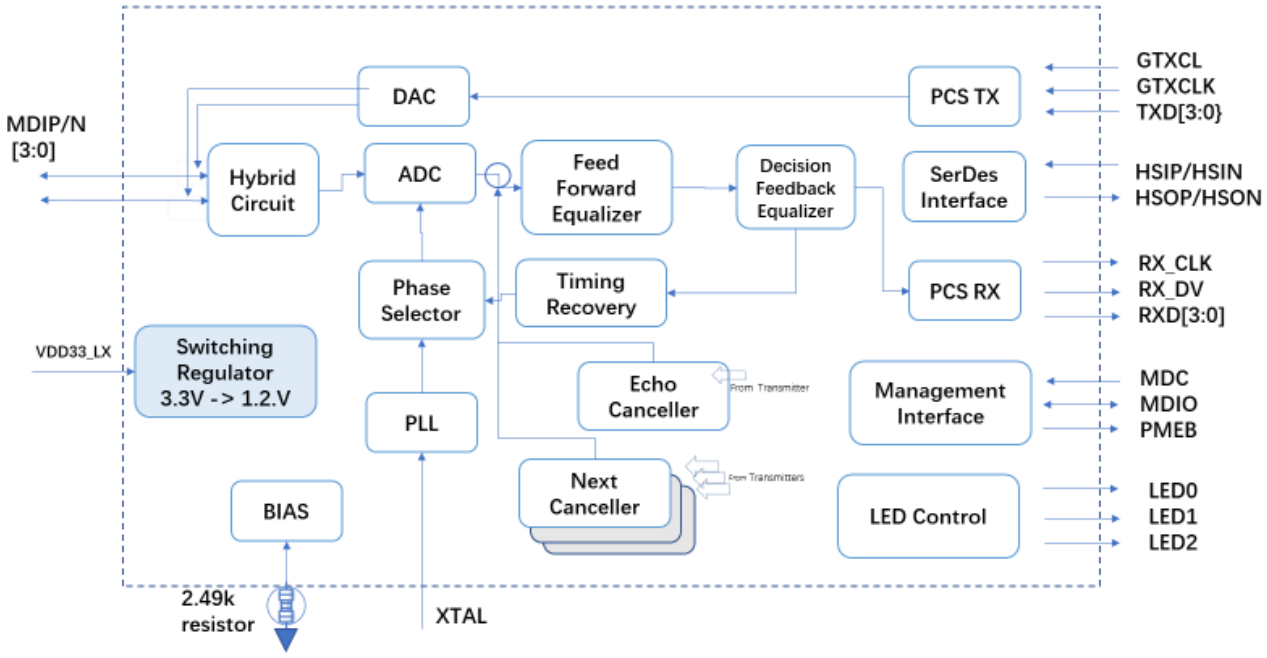


Figure 1. Blcok Diagram

3. Pin Assigment

3.1. YT8521SH/YT8521SC QFN48 6x6mm

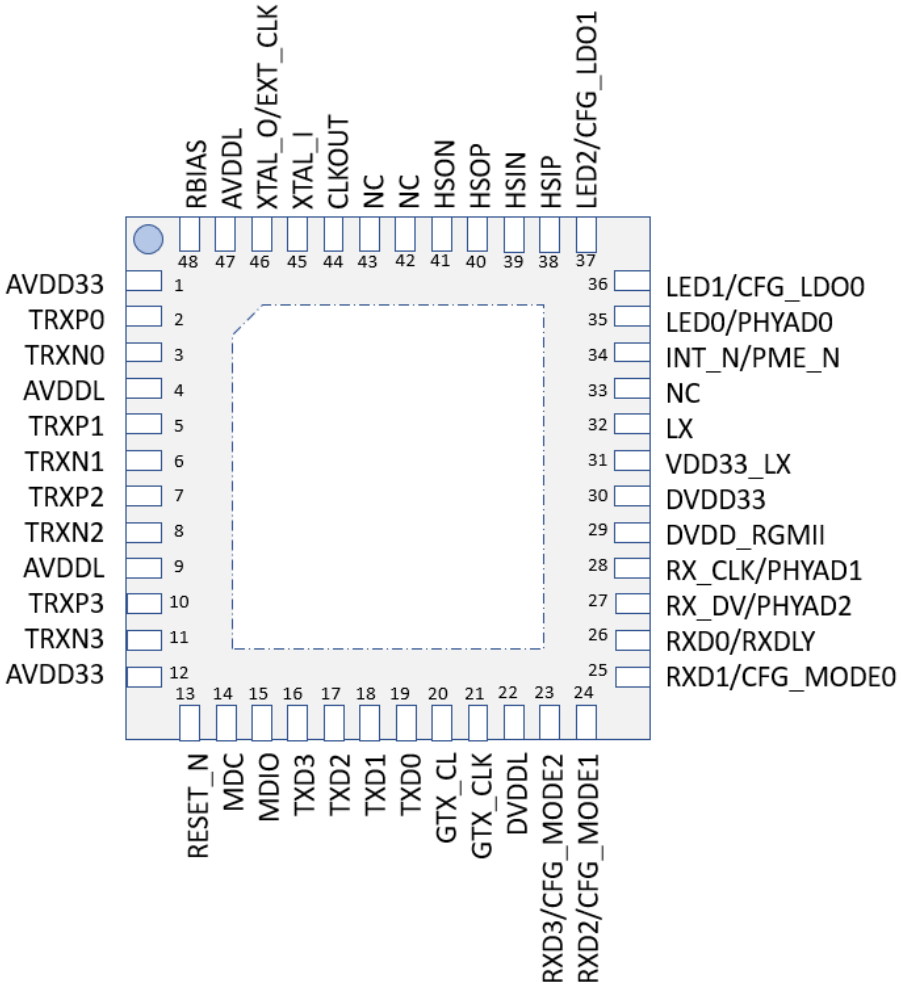


Figure 2. Pin Assigment Diagram

3.2. Pin Descriptions

Some pins have multiple functions.

Refer to the Pin Assignment figures for a graphical representation,

- I: Input
- O: Output
- P: Power
- PU: Internal pull up
- G: Ground
- LI: Latched Input During Power UP
- IO: Bidirectional Input and Output
- PD: Internal pull down
- OD: Open Drain

3.3. Pin Assignment

Table 1. Pin Assignment

No.	Pin Name	Type	Description
1	AVDD33	P	Analog Power 3.3V
2	TRXP0	IO	Media-dependent interface 0, 100Ω transmission line
3	TRXN0	IO	Media-dependent interface 0, 100Ω transmission line
4	AVDDL	P	Analog Power 1.2V.
5	TRXP1	IO	Media-dependent interface 1, 100Ω transmission line
6	TRXN1	IO	Media-dependent interface 1, 100Ω transmission line
7	TRXP2	IO	Media-dependent interface 2, 100Ω transmission line
8	TRXN2	IO	Media-dependent interface 2, 100Ω transmission line
9	AVDDL	P	Analog Power 1.2V.
10	TRXP3	IO	Media-dependent interface 3, 100Ω transmission line
11	TRXN3	IO	Media-dependent interface 3, 100Ω transmission line
12	AVDD33	P	Analog Power 3.3V
13	RESET_N	I,PU	System reset, active low. Requires an external pull-up resistor
14	MDC	I	Management data clock reference
15	MDIO	IO,PU	Management data, Pull up to 3.3/2.5/1.8 I/O respectively
16	TXD3	I	Transmit Data 3
17	TXD2	I	Transmit Data 2
18	TXD1	I	Transmit Data 1
19	TXD0	I	Transmit Data 0
20	GTX_CL	I	Transmit Control Signal from the MAC
21	GTX_CLK	I	RGMII transmit clock, 125 MHz digital. Adding a 22ohm damping resistor is recommended for EMI design near MAC side.
22	DVDDL	P	Digital power 1.2V
23	RXD3/CFG_MODE2	O/PD	Receive Data 3
24	RXD2/CFG_MODE1	O/PD	Receive Data 2
25	RXD1/CFG_MODE0	O/PD	Receive Data 1
26	RXD0/RXDLY	O/PU	Receive Data 0 add 2 ns delay to RXC for RXD latching
27	RX_DV/PHYAD2	O/PD	RGMII receive data valid. PHY address config [0]
28	RX_CLK/PHYAD1	O/PD	The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream. PHY address config [1]
29	DVDD_RGMII	P	RGMII IO power
30	DVDD33	P	Digital non-RGMII IO power , 3.3V
31	VDD33_LX	P	3.3V power supply for switching regulator
32	LX	P, O	Power inductor pin. Add an external 2.2 uH power inductor
33	NC	IO/PD	Reserved for internal use. Keep floating or external pull down. Do not external pull up.

34	INT_N/PME_N	O/OD/	This pin is shared by three functions, the default pin setting is INT_N. Keep this pin floating if either of the functions is not used. The pin type depends on function selected: 1. Interrupt (supports 3.3V pull up). Set low if the specified events occurred; active low. 2. Power Management Event (supports 3.3V pull up). Set low if received a magic packet, Wake-Up frame ,or wake up event; active low. Note 1: The behavior of INTB/PMEB is level-triggered. Note 2: The function of INTB/PMEB can be assigned by Ext 0xa00a bit 6. 1: Pin 34 functions as PME_N. 0: Pin 34 functions as INT_N (default)
35	LED0/PHYAD0	O/PU	LED0, PHY address config [0]
36	LED1/CFG_LDO0	O/PU	LED1, Voltage Selection for RGMII IO
37	LED2/CFG_LDO1	O/PD	LED2, Voltage Selection for RGMII IO
38	HSIP	I	SerDes Differential Input: 1.25GHz serial interfaces to receive data from an External device that supports the SGMII interface. The differential pair has an internal 100 ohm termination resistor.
39	HSIN	I	
40	HSOP	O	SerDes Differential Output: 1.25GHz serial interfaces to receive data from an External device that supports the SGMII interface. The differential pair has an internal 100 ohm termination resistor.
41	HSON	O	
42	NC	-	NC, keep floating or connect to GND
43	NC	G	NC, keep floating or connect to GND. Should not connect to VDD or be pulled up.
44	CLKOUT	O	1. Reference Clock Generated from Internal PLL.- This pin should be kept floating if the clock is not used by the MAC.” 2. UTP recovery receive clock for Sync Ethernet. 3. Fiber recovery receive clock for Sync Ethernet. 4. PTP synchronized clock output.,
45	XTAL_I	I	25MHz Crystal Input. Connect to GND if an external 25MHz oscillator drives XTAL_O/EXT_CLK pin.
46	XTAL_O/EXT_CLK	O	25Mhz Crystal Output. If a 25MHz oscillator is used, connect XTAL_O/EXT_CLK pin to the oscillator’s output.
47	AVDDL	P	Analog Power 1.2V.
48	RBIAS	O	Bias Resistor. An external 2.49 kΩ±1% resistor must be connected between the RBIAS pin and GND
49	GND	G	Exposed PAD

3.4. Transceiver Interface

Table 2. Transceiver Interface

No.	Pin Name	Type	Description
2	TRXP0	IO	Media-dependent interface 0, 100Ω transmission line
3	TRXN0	IO	Media-dependent interface 0, 100Ω transmission line
5	TRXP1	IO	Media-dependent interface 1, 100Ω transmission line
6	TRXN1	IO	Media-dependent interface 1, 100Ω transmission line
7	TRXP2	IO	Media-dependent interface 2, 100Ω transmission line
8	TRXN2	IO	Media-dependent interface 2, 100Ω transmission line
10	TRXP3	IO	Media-dependent interface 3, 100Ω transmission line
11	TRXN3	IO	Media-dependent interface 3, 100Ω transmission line

3.5. Clock

Table 3. Transceiver Interface

No.	Pin Name	Type	Description
44	CLKOUT	O	1. Reference Clock Generated from Internal PLL.- This pin should be kept floating if the clock is not used by the MAC." 2. UTP recovery receive clock for Sync Ethernet. 3. Fiber recovery receive clock for Sync Ethernet.
45	XTAL_I	I	25MHz Crystal Input. Connect to GND if an external 25MHz oscillator drives XTAL_O/EXT_CLK pin.
46	XTAL_O/ EXT_CLK	O	25Mhz Crystal Output. If a 25MHz oscillator is used, connect XTAL_O/EXT_CLK pin to the oscillator's output.

3.6. RGMII

Table 4. RGMII

No.	Pin Name	Type	Description
16	TXD3	I	Transmit Data 3
17	TXD2	I	Transmit Data 2
18	TXD1	I	Transmit Data 1
19	TXD0	I	Transmit Data 0
20	GTX_CL	I	Transmit Control Signal from the MAC
21	GTX_CLK	I	RGMII transmit clock, 125 MHz digital. Adding a 22ohm damping resistor is recommended for EMI design near MAC side.
23	RXD3	O/PD	Receive Data 3
24	RXD2	O/PD	Receive Data 2
25	RXD1	O/PD	Receive Data 1
26	RXD0	O/PD	Receive Data 0
28	RX_CLK		The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream.
27	RX_DV	O/PD	RGMII receive data valid

3.7. SerDes

Table 5. SerDes

No.	Pin Name	Type	Description
38	HSIP	I	SerDes Differential Input: 1.25GHz serial interfaces to receive data from an External device that supports the SGMII interface. The differential pair has an internal 100 ohm termination resistor.
39	HSIN	I	
40	HSOP	O	SerDes Differential Output: 1.25GHz serial interfaces to transfer data from an External device that supports the SGMII interface. The differential pair has an internal 100 ohm termination resistor.
41	HSON	O	

3.8. Reset

Table 6. Reset

No.	Pin Name	Type	Description
13	RESET_N	I,PU	System reset, active low. Requires an external pull-up resistor

3.9. Mode Selection

Table 7. Mode Selection

No.	Name	Type	Description
35	PHYAD0	O/PU	PHYADD[2:0]. PHY address config
28	PHYAD1	O/PD	
27	PHYAD2	O/PD	
26	RXDLY	O/PU	RGMII receiver clock timing control Pull-up to add 2ns delay to RXC to RXD latching
36	CFG_LDO0	O/PU	CFG_LDO[1:0], Voltage selection for RGMII I/O pad 2'b00: 3.3V 2'b01: 2.5V 2'b10: 1.8V 2'b11: reserved
37	CFG_LDO1	O/PD	
25	CFG_MODE0	O/PD	CFG_MODE[2:0]: Operation Mode Configuration. 3'b000: UTP <-> RGMII 3'b001: FIBER <->RGMII 3'b010: UTP/FIBER <-> RGMII (Media Auto Detection) 3'b011: UTP <-> SGMII 3'b100: SGMII (PHY side) <-> RGMII (MAC side), 3'b101: SGMII (MAC side) <->RGMII (PHY side) 3'b110: UTP <->FIBER (Media Conversion auto mode) 3'b111: UTP <-> FIBER (Media Conversion force mode)
24	CFG_MODE1	O/PD	
23	CFG_MODE2	O/PD	

3.10. LED

Table 8. LED

No.	Pin Name	Type	Description
35	LED0	O/PU	LED0, High = Link up at 10Mbps, Blinking= Transiting or Receiving
36	LED1	O/PU	LED1, High = Link up at 100Mbps, Blinking= Transiting or Receiving
37	LED2	O/PD	LED2, High = Link up at 1000Mbps, Blinking= Transiting or Receiving

3.11. Regulator and Reference

Table 9. Regulator and Reference

No.	Pin Name	Type	Description
48	RBIAS	O	Bias Resistor. An external 2.49 kΩ±1% resistor must be connected between the RBIAS pin and GND
32	LX	O	Power inductor pin. Add an external 2.2 uH power inductor directly

3.12. Power Related

Table 10. Power Related

No.	Pin Name	Type	Description
30	DVDD33	P,I	3.3V Power Digital non-RGMII I/O power
31	VDD33_LX	P,I	3.3V power for switching regulator
29	VDD_RGMII	P,O	Digital RGMII I/O, MDC, MDIO power. 3.3/2.5/1.8v adjusted by CFG_LDO[1:0]
22	DVDDL	P,I	Digital power 1.2V
1, 12	AVDD33	P,I	Analog Power 3.3V
4, 9, 47	AVDDL	P,I	Analog power 1.2V
42	NC	-	NC, keep floating or connect to GND
43	NC	G	NC, keep floating or connect to GND. Should not connect to VDD or be pulled up.
49	GND	G	Exposed PAD

3.13. Management

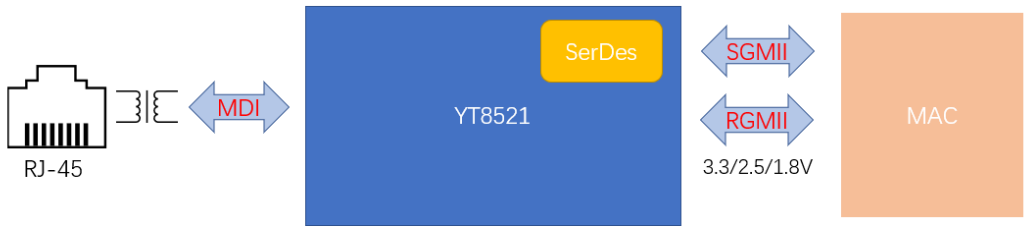
Table 11. Management

No.	Pin Name	Type	Description
14	MDC	I	Management data clock reference
15	MDIO	IO,PU	Management data, Pull up to 3.3/2.5/1.8 I/O respectively
34	INT_N/ PME_N	O/OD/	This pin is shared by three functions, the default pin setting is INT_N. Keep this pin floating if either of the functions is not used. The pin type depends on function selected: 1. Interrupt (supports 3.3V pull up). Set low if the specified events occurred; active low. 2. Power Management Event (supports 3.3V pull up). Set low if received a magic packet, Wake-Up frame ,or wake up event; active low. Note 1: The behavior of INTB/PMEB is level-triggered. Note 2: The function of INTB/PMEB can be assigned by Ext 0xa00a bit 6. 1: Pin 34 functions as PME_N. 0: Pin 34 functions as INT_N (default) Note 3:For more detailed INTB/PMEB usage.

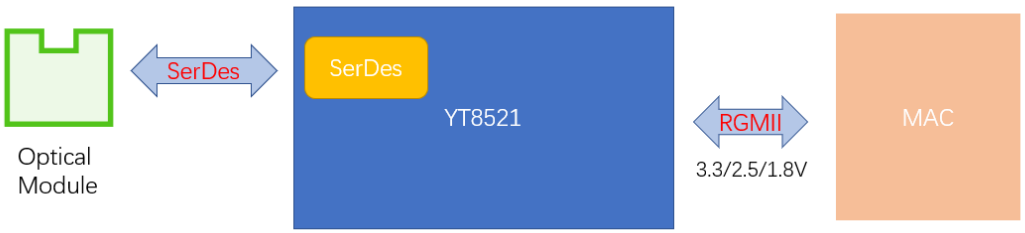
4. Function Description

4.1. Application Diagram

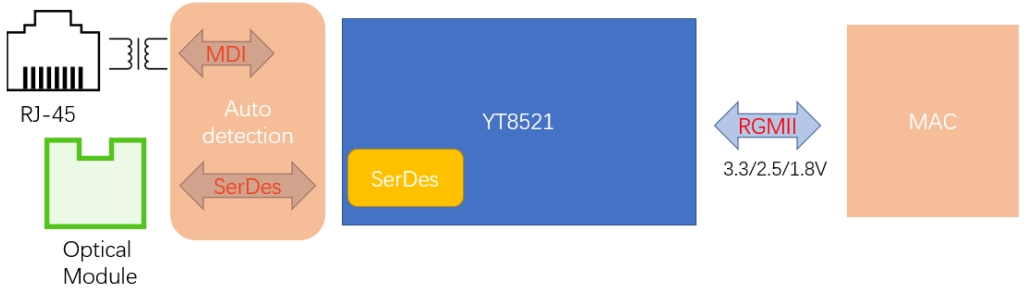
4.1.1. UTP (UTP<->RGMII / UTP<->SGMII) Application



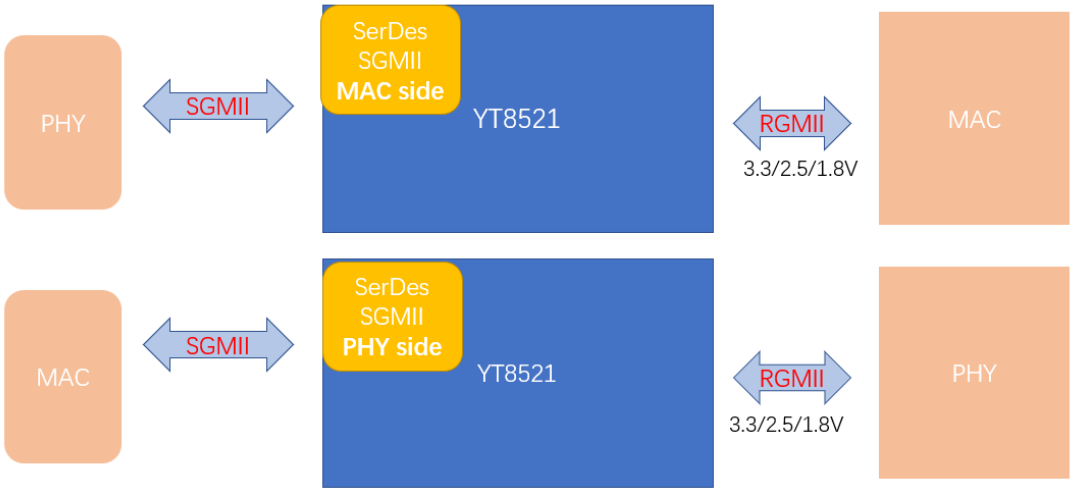
4.1.2. Fiber (FIBER<->RGMII) Application



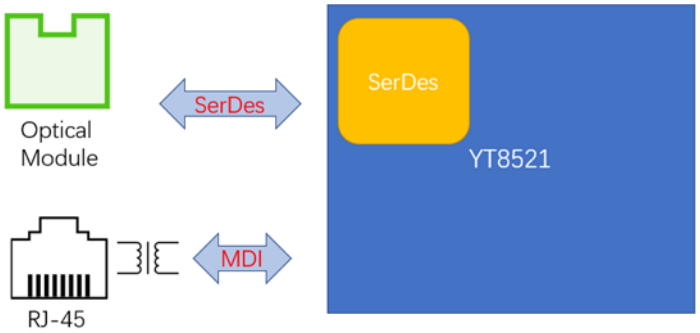
4.1.3. UTP/Fiber to RGMII (UTP/FIBER Media Auto Detection RGMII) Application



4.1.4. SGMII to RGMII (SGMII <->RGMII Bridge Mode) Application



4.1.5. Fiber to UTP (UTP<->FIBER Media Converter) Application



4.2. Transmit Functions

4.2.1. Transmit Encoder Modes Encoder Mode Description

4.2.1.1. 1000 BASE-T

In 1000 BASE-T mode, the YT8521SH/YT8521SC scrambles transmit data bytes from the MAC interfaces to 8-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5 cable.

4.2.1.2. 100 BASE-TX

In 100 BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.

4.2.1.3. 10 BASE-TE

In 10 BASE-Te mode, the YT8521 transmits and receives Manchester-encoded data.

4.3. Receive Functions

4.3.1. Receive Decoder Modes

4.3.1.1. 1000 BASE-T

In 1000 BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately and data is output to the MAC interfaces.

4.3.1.2. 100 BASE-TX

In 100 BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/ 4B decoded to 4-bit data. This output runs to the MII receive data pins after data stream delimiters have been translated.

4.3.1.3. 10 BASE-TE

In 10 BASE-Te mode, the recovered 10 BASE-Te signal is decoded from Manchester then aligned.

4.4. Hyper range

Hyper-range is the motor-comm proprietary mode in extended cable reach application up to 400m in 100M mode. HR-100 is 100Mbps Mode.

4.5. Echo Canceller

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects back as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, also result in drastic SNR degradation on the receive signal. The YT8521SH/YT8521SC device implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

4.6. NEXT Canceller

The 1000 BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled together, significant high frequency crosstalk occurs between adjacent pairs in the bundle. The YT8521SH/YT8521SC device uses three parallel NEXT cancellers on each receive channel to cancel high frequency crosstalk. The YT8521SH/YT8521SC cancels NEXT by subtracting an estimate of these signals from the equalizer output.

4.7. Baseline Wander Canceller

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. Baseline wander is more problematic in the 1000 BASE-T environment than in 100 BASE- TX due to the DC baseline shift in the transmit and receive signals. The YT8521 device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

4.8. Digital Adaptive Equalizer

The digital adaptive equalizer removes inter- symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best optimized signal-to-noise (SNR) ratio.

4.9. Management interface

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 25 MHz.

4.10. Auto-Negoitation

The YT8521SH/YT8521SC negotiates its operation mode using the auto negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto negotiation supports choosing the mode of operation automatically by comparing its own abilities and received abilities from link partner. The advertised abilities include:

a) Speed: 10/100/1000Mbps

b) Duplex mode: full duplex and/or half duplex

Auto negotiation is initialized when the following scenarios happen:

a) Power-up/Hardware/Software reset

b) Auto negotiation restart

c) Transition from power-down to power up

d) Link down

Auto negotiation is enabled for YT8521SH/YT8521SC by default, and can be disable by hardware or software control.

4.11. LDS (Link discovey signaling)

YT8521SH/YT8521SC supports hyper range, which uses link discovery signaling (LDS) instead of auto negotiation since the extended cable reach attenuates the auto negotiation link pulses. LDS is an extended reach signaling scheme and protocol, which is used to

a) Master/Slave assignment

b) Estimate cable length

c) Confirm pair number and pair connectivity ordering

d) Choose highest common operation mode

IEEE-compliant PHYs will ignore LDS signal since its frequency is less than 2MHz according to IEEE802.3 clause 14. If the link partner is an IEEE legacy ethernet PHY, YT8521SH/YT8521SC can detect the standard NLP, FLP, MLT-3 IDLE signal, or 100BASE-T4 signal, and then transits LDS mode into Clause 28 auto negotiation mode.

Forcing pair number and speed mode is also supported. The same forcing must be done at both ends of the link.

The default of LDS is disabled, and should be enabled before using this feature.

4.12. Polarity detection and auto correction

YT8521SH/YT8521SC can detect and correct two types of cable errors: swapping of pairs within the UTP cable and swapping of wires within a pair.

4.13. Energy Efficient Ethernet (EEE)

EEE is IEEE 802.3az, an extension of the IEEE 802.3 standard. EEE defines support for the PHY to operate in Low Power Idle (LPI) mode which, when enabled, supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY's circuitry and save power.

YT8521SH/YT8521SC also helps legacy MAC without EEE ability to work as a complete EEE power saving system.

4.14. Synchronous Ethernet (Sync-E)

YT8521SH/YT8521SC provides Synchronous Ethernet (Sync-E) support when the device is operating in 1000Base-T, 100Base-TX, 1000Base-X, and 100Base-FX on the transmission media. The CLKOUT pin can be assigned to output the recovered clock.

The recovery clock for Sync-E can be either a 125MHz or 25MHz clock.

When the PHY is in SLAVE mode, the CLKOUT will output the recoverd clock from the MDI. If the device is in MASTER mode, the CLKOUT will output the clock based on the local free run PLL.

5. Operational Description

5.1. Reset

YT8521SH/YT8521SC have a hardware reset pin(RESET_N) which is low active. RESET_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up.

RESET_N is also used as enable for power on strapping. During RESET_N is active, YT8521SH/YT8521SC latches input value on RX_DV and RXD[3:0] as strapping[4:0]. Strapping[4:0] is used as configuration information which provides flexibility in application without mdio access.

YT8521SH/YT8521SC also provides two software reset control registers which are used to reset all internal logic except some mdio configuration registers. For detailed information about what register will be reset by software reset, please refer to register table. Configure bit 15 of lds mii register(address 0x0) or mii register(address 0x0) to 1 to enable software reset. These two bits are self-clear after reset process is done.

Table 12. Reset Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
T1	The duration from all powers steady to reset signal release to high	10	-	-	ms
T2	The duration of reset signal remain low timing	10	-	-	ms

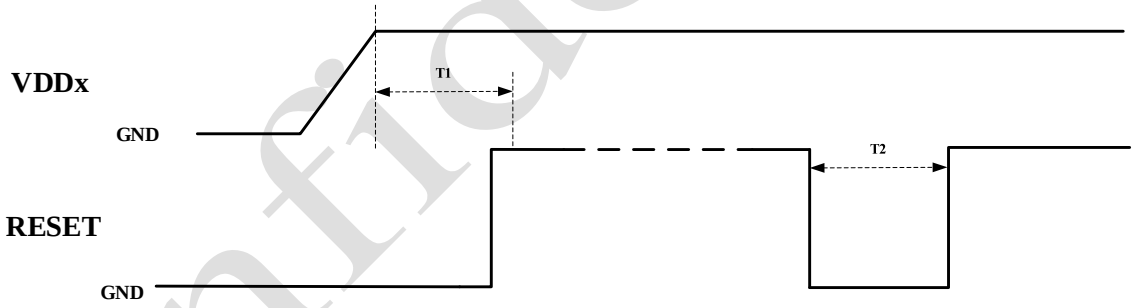


Figure 3. Reset Timing Diagram

5.2. PHY Address

For YT8521SH/YT8521SC, Strapping PHYAD[2:0] is used to generate phy address.

YT8521SH/YT8521SC always response to phy address 0. It also has another broadcast phy address which is configurable through mdio. Bit[4:0] of extended register(address 0x0) is broadcast phy address and its default value is 5'b11111. Bit[5] of extended register(address 0x0) is enable control for broadcast phy address and its default value is 1'b1.

5.3. RGMII interface

Reduced gigabit media independent interface is a subset of GMII which is used for gigabit Ethernet. For 100M/10M application, RGMII is similar to MII. The only difference is that tx_er/rx_er is transmitted by tx_en/rx_dv on the falling edge of clock. TXD[3:0] and RXD[3:0] will be duplicated on both rising and falling edge of clock. For 100M application, TXC and RXC are 25MHz; for 10M application, TXC and RXC are 2.5MHz.

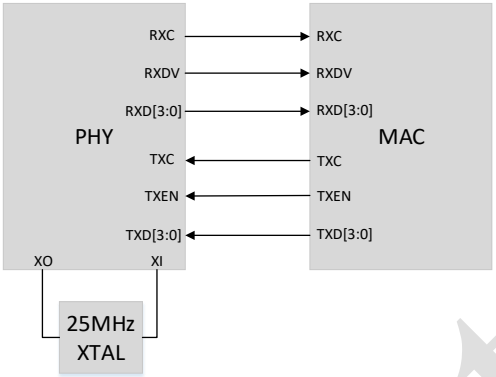


Figure 4. Connection Diagram of RGMII

5.4. SQI

YT8521SH/YT8521SC provides a method to monitor quality of link.

By reading extended register mse(address 0h1005), we can obtain SNR during following steps.

a) Read register mse[14:0]

b) Calculate SNR = 10*log10(32768/(3*mse))

c) Average over 200 readings A= avg(SNR)

d) Rank the link quality

i. SQI = 5 when A > 23

ii. SQI = 4 when 18 < A < 23

iii. SQI = 3 when 15 < A < 18

iv. SQI = 2 when 15 < A < 18

v. SQI = 1 when 11 < A < 14

5.5. Loopback mode

There are three loopback modes in YT8521SH/YT8521SC

5.5.1. Digital Loopback

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the YT8521SH/YT8521SC device.

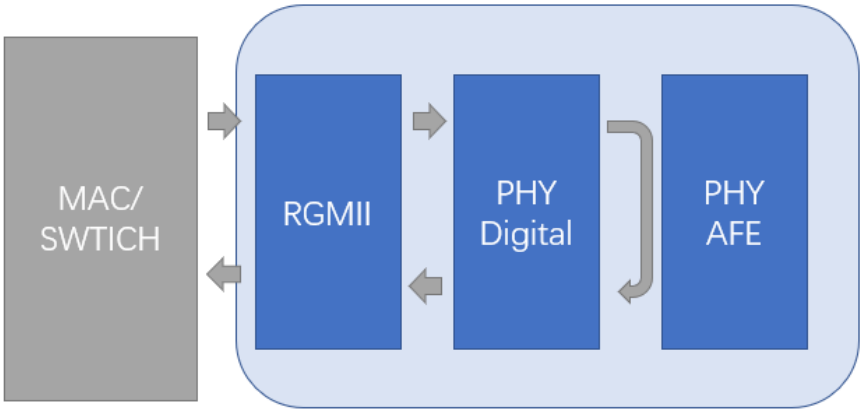


Figure 5. Digital Loopback

1000M loopback: write register 0x0 = 0x4140 to enable 1000M digital loopback.

100M loopback: write register 0x0 = 0x6100 to enable 100M digital loopback.

10M loopback: write register 0x0 = 0x4100 to enable 10M digital loopback.

5.5.2. External loopback

External cable loopback loops Tx to Rx through a complete digital and analog path and an external cable, thus testing all the digital data paths and all the analog circuits. Figure shows a block diagram of external cable loopback.

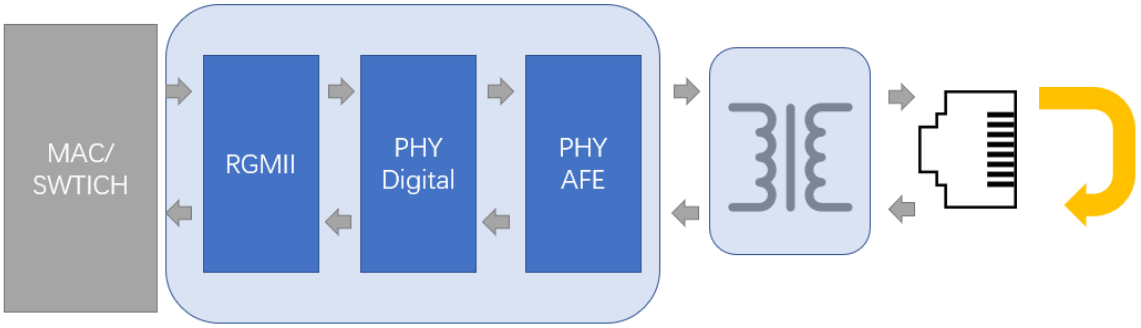


Figure 6. External Loopback

5.5.3. Remote PHY loopback

The Remote loopback connects the MDI receive path to the MDI transmit path, near the RGMII interface, thus the remote link partner can detect the connectivity in the resulting loop. Figure below, shows the path of the remote loopback.

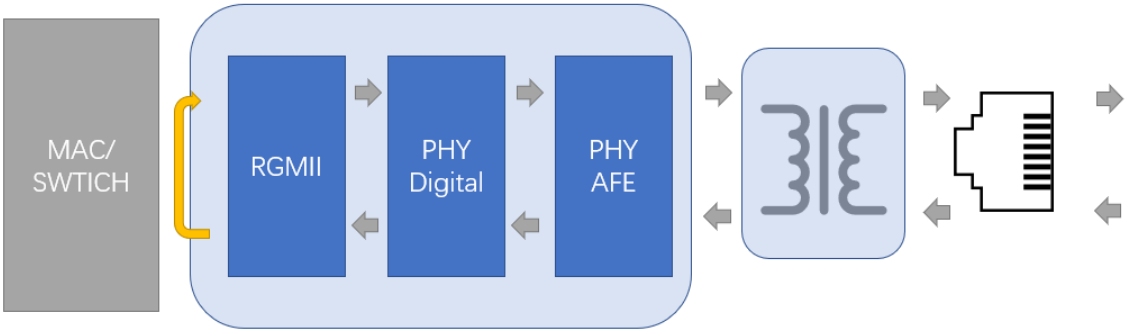


Figure 7. Remote PHY Loopback

5.6. LED

The LED interface can either be controlled by the PHY or controlled manually, independent of the state of the PHY. Three status LEDs are available. These can be used to indicate operation speed, duplex mode, and link status. The LEDs can be programmed to different status functions from their default value. They can also be controlled directly from the register interface.

5.7. Auto Negotiation

When auto negotiation is enabled, YT8521SH/YT8521SC operation mode is based on the negotiation results, including speed and duplex mode. Registers configurations are shown as:

Register Type	Register Address	Write Value	Comments
Extended	16'h0100	16'h0006	Bit2: 1'b1, Access IEEE MII regs
MII	16'h0000		Bit12: 1'b1, enable auto negotiation

Table: Enable auto negotiation

Register Type	Register Address	Write Value	Comments
Extended	16'h0100	16'h0006	Bit2: 1'b1, Access IEEE MII regs
MII	16'h0000		Bit9: 1'b1, restart auto negotiation

Table: Restart auto negotiation

Register Type	Register Address	Write Value	Comments
Extended	16'h0100	16'h0006	Bit2: 1'b1, Access IEEE MII regs
MII	16'h0001		Bit5: 1'b1, AN complete; 1'b0, AN not complete Bit3: 1'b1, support AN; 1'b0, not support AN Bit2: 1'b1, Link up; 1'b0, link down
MII	16'h0011		Bit15-14: 2'b00, 10Mbps; 2'b01: 100Mbps Bit5: 1'b1, link is downgrade; 1'b0, link is not downgrade

Table: Auto negotiation status

When auto negotiation is disabled, forcing speed and duplex mode is also support. Forcing 10BASE-T has been discussed in the LDS part. Registers configuration for Forcing 100BASE-TX is shown as:

Register Type	Register Address	Write Value	Comments
Extended	16'h0100	16'h0006	Bit2: 1'b1, Access IEEE MII regs
MII	16'h0000		Bit12: 1'b0, disable auto negotiation Bit6,13: 2'b01, 100Mbps Bit8: 1'b1, full duplex

Table: Forcing 100BASE-TX

During auto negotiation, YT8521SH/YT8521SC supports automatic MDI crossover by detecting and correcting external crossover cable. If the link partner also supports automatic MDI crossover, only one

device performs the crossover according to IEEE 802.3 Clause 40.4.4. YT8521SH/YT8521SC also supports forcing MDI/MDIX mode. Registers configurations are shown as:

Register Type	Register Address	Write Value	Comments
Extended	16'h0100	16'h0006	Bit2: 1'b1, Access IEEE MII regs
MII	16'h0010		Bit6-5: 2'b00, forcing MDI; 2'b01, forcing MDIX; 2'b11, automatic MDI crossover

Table: MDI/MDI-X configuration

5.8. Power Supplies

The YT8521SH/YT8521SC device requires only one external power supply: 3.3 V. Inside the chip there is a 3.3V rail, 1.2V rail, 2.5V or 1.8V rail.

YT8521SH/YT8521SC integrates a switch regulator which converts 3.3V to 1.2V at a high-efficiency for core power rail. (It is optional for an external regulator to provide this core voltage).

6. Register Overview

MII Management Interface Clause 22 Register Programming

The YT8521SH/YT8521SC transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification.

The MII management interface registers are written and read serially, using the MDIO and MDC pins.

A clock of up to 25 MHz must drive the MDC pin of the YT8521SH/YT8521SC. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

6.1. Common Register

6.1.1. SMI_SDS_PHY (EXT_0xA000)

Table 13. SMI_SDS_PHY (EXT_0xA000)

Bit	Symbol	Access	Default	Description
15:2	Reserved	RO	0x0	Reserved
1	Smi_sds_phy	RW	0x0	to control access whether phy register or sds register. 1 to access sds; 0 to access phy. Default value depend on chip mode. When phy exsit, default 0; else default 1
0	Reserved	RO	0x0	Reserved

6.1.2. LED_GENERAL_CFG (EXT_0xA00B)

Table 14. LED_GENERAL_CFG (EXT_0xA00B)

Bit	Symbol	Access	Default	Description
15	Col_blk_sel	RW	0x1	1 = when collision happens, and related LEDn cfg (n is 0/1/2) register's bit3 led_col_blk_en is 1, LED blink at Blink Mode2; 0 = when collision happens, and related LEDn cfg (n is 0/1/2) register's bit3 led_col_blk_en is 1, LED blink at Blink Mode1. LED could blinks at different frequency in Blink Mode1 and Blink Mode2. Refer to EXT A00F[3:0] for the Blink Mode2 and Blink Mode1.
14	Jabber_led_dis	RW	0x1	1 = when 10Mb/s Jabber happens, LED will not blink;
13	Lpbk_led_dis	RW	0x1	1 = In internal loopback mode, LED will not blink;
12	Dis_led_an_try	RW	0x0	1: LED will be ON when auto-negotiation is at LINK_GOOD_CHECK status, in which status, the link is not up already.
11:9	Reserved	RO	0x0	Reserved
8	Led_2_force_en	RW	0x0	1 = enable LED2 force mode.
7:6	Led_2_force_mode	RW	0x0	Valid when bit8 is set. 00: force LED OFF; 01: force LED ON; 10: force LED Blink at Blink Mode1; 11: force LED Blink at Blink Mode2. LED could blinks at different frequency in Blink Mode1 and Blink Mode2. Refer to EXT A00F[3:0] for the Blink Mode2 and Blink Mode1.
5	Led_1_force_en	RW	0x0	1 = enable LED1 force mode.
4:3	Led_1_force_mode	RW	0x0	Valid when bit5 is set. Refer EXT A00B[7:6] for the force mode description.
2	Led_0_force_en	RW	0x0	1 = enable LED0 force mode.
1:0	Led_0_force_mode	RW	0x0	Valid when bit5 is set. Refer EXT A00B[7:6] for the force mode description.

6.1.3. LED0_CFG (EXT_0xA00C)

Table 15. LED0_CFG (EXT_0xA00C)

Bit	Symbol	Access	Default	Description

15:14	Led_src_sel_0	RW	0x0	select the source of internal signals controlling LED0; 2'b00: phy; 2'b01: serdes; 2'b10: phy and serdes; 2'b11: phy or serdes. Default value of LED0 cfg depends on the strapping of chip mode:
13	Led_act_blk_ind_0	RW	0x0	When traffic is present, make LED0 BLINK no matter the previous LED0 status is ON or OFF, or make LED0 blink only when the previous LED0 is ON.
12	Led_fdx_on_en_0	RW	0x0	1: If BLINK status is not activated, when PHY link up and duplex mode is full duplex, LED0 will be ON.
11	Led_hdx_on_en_0	RW	0x0	If BLINK status is not activated, when PHY link up and duplex mode is half duplex,
10	Led_txact_blk_en_0	RW	0x1	1: If bit13 is 1, or bit13 is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and TX is active,
9	Led_rxact_blk_en_0	RW	0x1	If bit13 is 1, or bit13 is 0 and ON at certain speed or duplex more is/are activated, when PHY link up and RX is active,
8	Led_txact_on_en_0	RW	0x0	1 = if BLINK status is not activated, when PHY link up and TX is active, make LED0 ON at least 10ms;
7	Led_rxact_on_en_0	RW	0x0	1 = if BLINK status is not activated, when PHY link up and RX is active, make LED0 ON at least 10ms;
6	Led_gt_on_en_0	RW	0x0	1 = if BLINK status is not activated, when PHY link up and speed mode is 1000Base-T, make LED0 ON;
5	Led_ht_on_en_0	RW	0x0	1 = if BLINK status is not activated, when PHY link up and speed mode is 100Base_TX, make LED0 ON;
4	Led_bt_on_en_0	RW	0x1	1 = if BLINK status is not activated, when PHY link up and speed mode is 10Base-T, make LED0 ON;
3	Led_col_blk_en_0	RW	0x0	1 = if PHY link up and collision happen, make LED0 BLINK;
2	Led_gt_blk_en_0	RW	0x0	1 = if PHY link up and speed mode is 1000Base-T, make LED0 BLINK;
1	Led_ht_blk_en_0	RW	0x0	1 = if PHY link up and speed mode is 100Base-T, make LED0 BLINK;
0	Led_bt_blk_en_0	RW	0x0	1 = if PHY link up and speed mode is 10Base-T, make LED0 BLINK;

6.1.4. LED1_CFG (EXT_0xA00D)

Table 16. LED1_CFG (EXT_0xA00D)

Bit	Symbol	Access	Default	Description
15:14	Led_src_sel_1	RW	0x0	Same logic as LED0 control.
13	Led_act_blk_ind_1	RW	0x0	Same logic as LED0 control.
12	Led_fdx_on_en_1	RW	0x0	Same logic as LED0 control.
11	Led_hdx_on_en_1	RW	0x0	Same logic as LED0 control.
10	Led_txact_blk_en_1	RW	0x1	Same logic as LED0 control.
9	Led_rxact_blk_en_1	RW	0x1	Same logic as LED0 control.
8	Led_txact_on_en_1	RW	0x0	Same logic as LED0 control.
7	Led_rxact_on_en_1	RW	0x0	Same logic as LED0 control.
6	Led_gt_on_en_1	RW	0x0	Same logic as LED0 control.
5	Led_ht_on_en_1	RW	0x1	Same logic as LED0 control.

4	Led_bt_on_en_1	RW	0x0	Same logic as LED0 control.
3	Led_col_blk_en_1	RW	0x0	Same logic as LED0 control.
2	Led_gt_blk_en_1	RW	0x0	Same logic as LED0 control.
1	Led_ht_blk_en_1	RW	0x0	Same logic as LED0 control.
0	Led_bt_blk_en_1	RW	0x0	Same logic as LED0 control.

6.1.5. LED2_CFG (EXT_0xA00E)

Table 17. LED2_CFG (EXT_0xA00E)

Bit	Symbol	Access	Default	Description
15:14	Led_src_sel_2	RW	0x0	Same logic as LED0 control.
13	Led_act_blk_ind_2	RW	0x0	Same logic as LED0 control.
12	Led_fdx_on_en_2	RW	0x0	Same logic as LED0 control.
11	Led_hdx_on_en_2	RW	0x0	Same logic as LED0 control.
10	Led_txact_blk_en_2	RW	0x1	Same logic as LED0 control.
9	Led_rxact_blk_en_2	RW	0x1	Same logic as LED0 control.
8	Led_txact_on_en_2	RW	0x0	Same logic as LED0 control.
7	Led_rxact_on_en_2	RW	0x0	Same logic as LED0 control.
6	Led_gt_on_en_2	RW	0x1	Same logic as LED0 control.
5	Led_ht_on_en_2	RW	0x0	Same logic as LED0 control.
4	Led_bt_on_en_2	RW	0x0	Same logic as LED0 control.
3	Led_col_blk_en_2	RW	0x0	Same logic as LED0 control.
2	Led_gt_blk_en_2	RW	0x0	Same logic as LED0 control.
1	Led_ht_blk_en_2	RW	0x0	Same logic as LED0 control.
0	Led_bt_blk_en_2	RW	0x0	Same logic as LED0 control.

6.1.6. LED_BLINK_CFG (EXT_0xA00F)

Table 18. LED_BLINK_CFG (EXT_0xA00F)

Bit	Symbol	Access	Default	Description
15:7	Reserved	RO	0x0	Reserved
6:4	Led_duty	RW	0x0	Select duty cycle of Blink: 000: 50% ON and 50% OFF; 001: 67% ON and 33% OFF; 010: 75% ON and 25% OFF; 011: 83% ON and 17% OFF; 100: 50% ON and 50% OFF; 101: 33% ON and 67% OFF; 110: 25% ON and 75% OFF; 111: 17% ON and 83% OFF.
3:2	Freq_sel_2	RW	0x1	Select frequency of Blink Mode2: 00: 32Hz; 01: 16Hz; 10: 8Hz; 11: 4Hz.
1:0	Freq_sel_1	RW	0x2	Select frequency of Blink Mode1: 00: 32Hz; 01: 16Hz; 10: 8Hz; 11: 4Hz.

6.1.7. SyncE_CFG (EXT_0xA012)

Table 19. SyncE_CFG (EXT_0xA012)

Bit	Symbol	Access	Default	Description
15:7	Reserved	RO	0x0	Reserved
6	Phy_do_fib	RW	0x1	1=Phy shut off until fiber link up
5	En_sync_e	RW	0x0	enable sync e clock output
4	En_sync_e_during_lnkdn	RW	0x0	always output sync e clock even when link is down
3	Clk_fre_sel	RW	0x1	1'b1: output 125m clock; 1'b0: output 25m clock
2:1	Clk_src_sel	RW	0x0	select clock source of synce. 2'b00: pll clock; 2'b01: utp recovered rx clock; 2'b10: sds recovered rx clock; 2'b11: ptp clk in
0	Ptp_clk_to_sds_sel	RW	0x0	1=output transmit clock to synce clock, used for template test; 1'b0=output ptpin clock to synce clock

6.2. Phy MII Register

6.2.1. Basic Control Register (0x00)

Table 20. Basic Control Register (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 0: Normal operation 1: PHY reset
14	Loopback	RW SWC	0x0	Internal loopback control 1'b0: disable loopback 1'b1: enable loopback
13	Speed_Selection(LSB)	RW	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero. Bit6 bit13 1 1 = Reserved 1 0 = 1000Mb/s 0 1 = 100Mb/s 0 0 = 10Mb/s
12	Autoneg_En	RW	0x1	1: to enable auto-negotiation; 0: auto-negotiation is disabled.
11	Power_down	RW SWC	0x0	1 = Power down 0 = Normal operation When the port is switched from power down to normal operation, software reset and Auto-Negotiation are performed even bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user.
10	Isolate	RW SWC	0x0	Isolate phy from RGMII/SGMII/FIBER. 1'b0: Normal mode 1'b1: Isolate mode
9	Re_Autoneg	RW SC SWS	0x0	Auto-Negotiation automatically restarts after hardware or software reset regardelss of bit[9] RESTART. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Duplex_Mode	RW	0x1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0. 1 = Full Duplex 0 = Half Duplex
7	Collision_Test	RW SWC	0x0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted. 1 = Enable COL signal test 0 = Disable COL signal test
6	Speed_ Selection(MSB)	RW	0x1	See bit13.
5:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

6.2.2. Basic Status Register (0x01)

Table 21. Basic Status Register (0x01)

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	0x0	PHY doesn't support 100BASE-T4
14	100Base-X_Fd	RO	0x1	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	0x1	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	0x1	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	0x1	PHY supports 10Mbps_Hd
10	100Base-T2_Fd	RO	0x0	PHY doesn't support 100Base-T2_Fd
9	100Base-T2_Hd	RO	0x0	PHY doesn't support 100Base-T2_Hd
8	Extended_Status	RO	0x1	Whether support EXTended status register in 0Fh 0: Not supported 1: Supported
7	Unidirect_Ability	RO	0x0	1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established 1'b1: PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	0x1	1'b0: PHY will not accept management frames with preamble suppressed 1'b1: PHY will accept management frames with preamble suppressed
5	Autoneg_Complete	RO SWC	0x0	1'b0: Auto-negotiation process not completed 1'b1: Auto-negotiation process completed
4	Remote_Fault	RO RC SWC L	0x0	1'b0: no remote fault condition detected 1'b1: remote fault condition detected
3	Autoneg_Ability	RO	0x1	1'b0: PHY not able to perform Auto-negotiation 1'b1: PHY able to perform Auto-negotiation
2	Link_Status	RO LL SWC	0x0	Link status 1'b0: Link is down 1'b1: Link is up
1	Jabber_Detect	RO RC LH SW	0x0	10Baset jabber detected. It would assert if TX activity lasts longer than 42ms. 1'b0: no jabber condition detected 1'b1: Jabber condition detected.
0	Extended_Capability	RO	0x1	To indicate whether support EXTended registers, to access from address register 1Eh and data register 1Fh 1'b0: Not supported 1'b1: Supported

6.2.3. PHY Identification Register1 (0x02)

Table 22. PHY Identification Register1 (0x02)

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	0x0	Bits 3 to 18 of the Organizationally Unique Identifier

6.2.4. PHY Identification Register2 (0x03)

Table 23. PHY Identification Register2 (0x03)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	0x0	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0x11	6 bits manufacturer's type number
3:0	Revision_No	RO	0xa	4 bits manufacturer's revision number

6.2.5. Auto-Negotiation Advertisement (0x04)

Table 24. Auto-Negotiation Advertisement (0x04)

Bit	Symbol	Access	Default	Description
15	NEXT_Page	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down If 1000BASE-T is advertised, the required next pages are automatically transmitted. This bit must be set to 0 if no additional next page is needed. 1 = Advertise 0 = Not advertised
14	Ack	RO	0x0	Always 0.
13	Remote_Fault	RW	0x0	1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
12	Extended_NEXT_Page	RW	0x1	Extended nEXT page enable control bit 1 = Local device supports transmission of extended next pages 0 = Local device does not support transmission of extended next pages.
11	Asymmetric_Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause
10	Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: This bit is updated immediately after the writing operation; however the configuration does not

				take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
9	100BASE-T4	RO	0x0	1 = Able to perform 100BASE-T4 0 = Not able to perform 100BASE-T4 Always 0
8	100BASE-TX_Full_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
7	100BASE-TX_Half_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
6	10BASE-Te_Full_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
5	10BASE-Te_Half_Duplex	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:

				• Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
4:0	Selector_Field	RW	0x1	Selector Field mode. 00001 = IEEE 802.3

6.2.6. Auto-Negotiation Link Partner Ability (0x05)

Table 25. Auto-Negotiation Link Partner Ability (0x05)

Bit	Symbol	Access	Default	Description
15	1000Base-X_Fd	RO SWC	0x0	Received Code Word Bit 15 1 = Link partner is capable of next page 0 = Link partner is not capable of next page
14	ACK	RO SWC	0x0	Acknowledge. Received Code Word Bit 14 1 = Link partner has received link code word 0 = Link partner has not received link code word
13	REMOTE_FAULT	RO SWC	0x0	Remote Fault. Received Code Word Bit 13 1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault
12	RESERVED	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 12
11	ASYMMETRIC_PAUSE	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
10	PAUSE	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 10 1 = Link partner supports pause operation 0 = Link partner does not support pause operation
9	100BASE-T4	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 9 1 = Link partner supports 100BASE-T4 0 = Link partner does not support100BASE-T4
8	100BASE-TX_FULL_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 8 1 = Link partner supports 100BASE-TX full-duplex 0 = Link partner does not support 100BASE-TX full-duplex
7	100BASE-TX_HALF_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 7 1 = Link partner supports 100BASE-TX half-duplex 0 = Link partner does not support 100BASE-TX half-duplex

6	10BASE-Te_FULL_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 6 1 = Link partner supports 10BASE-Te full-duplex 0 = Link partner does not support 10BASE-Te full-duplex
5	10BASE-Te_HALF_DUPLEX	RO SWC	0x0	Technology Ability Field. Received Code Word Bit 5 1 = Link partner supports 10BASE-Te half-duplex 0 = Link partner does not support 10BASE-Te half-duplex
4:0	SELECTOR_FIELD	RO SWC	0x0	Selector Field Received Code Word Bit 4:0

6.2.7. Auto-Negotiation Expansion Register (0x06)

Table 26. 6.2.7. Auto-Negotiation Expansion Register (0x06)

Bit	Symbol	Access	Default	Description
15:5	Reserved	RO	0x0	Reserved
4	Parallel Detection fault	RO RC LH SW	0x0	1 = Fault is detected 0 = No fault is detected
3	Link partner nEXT page able	RO LH SWC	0x0	1 = Link partner supports NEXT page 0 = Link partner does not support next page
2	Local NEXT Page able	RO	0x1	1 = Local Device supports NEXT Page 0 = Local Device does not Next Page
1	Page received	RO RC LH	0x0	1 = A new page is received 0 = No new page is received
0	Link Partner Auto negotiation able	RO	0x0	1 = Link partner supports auto-negotiation 0 = Link partner does not support auto-negotiation

6.2.8. Auto-Negotiation NEXT Page Register (0x07)

Table 27. Auto-Negotiation NEXT Page Register (0x07)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RW	0x0	Transmit Code Word Bit 15 1 = The page is not the last page 0 = The page is the last page
14	Reserved	RO	0x0	Transmit Code Word Bit 14
13	Message page mode	RW	0x1	Transmit Code Word Bit 13 1 = Message Page 0 = Unformatted Page
12	Ack2	RW	0x0	Transmit Code Word Bit 12 1 = Comply with message 0 = Cannot comply with message
11	Toggle	RO	0x0	Transmit Code Word Bit 11 1 = This bit in the previously exchanged Code Word is logic 0 0 = The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message/Unformatte	RW	0x1	Transmit Code Word Bits [10:0]. These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code

				Field when bit[13] is set to 0.

6.2.9. Auto-Negotiation Link Partner Received NEXT Page Register (0x08)

Table 28. Auto-Negotiation Link Partner Received NEXT Page Register (0x08)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RO	0x0	Received Code Word Bit 15 1 = This page is not the last page 0 = This page is the last page
14	Reserved	RO	0x0	Received Code Word Bit 14
13	Message page mode	RO	0x0	Received Code Word Bit 13 1 = Message Page 0 = Unformatted Page
12	Ack2	RO	0x0	Received Code Word Bit 12 1 = Comply with message 0 = Cannot comply with message
11	Toggle	RO	0x0	Received Code Word Bit 11 1 = This bit in the previously exchanged Code Word is logic 0 0 = The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message/Unformatte	RO	0x0	Received Code Word Bit 10:0 These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

6.2.10. MASTER-SLAVE control register (0x09)

Table 29. MASTER-SLAVE control register (0x09)

Bit	Symbol	Access	Default	Description
15:13	Test mode	RW	0x0	The TX_TCLK signals from the RX_CLK pin is for jitter testing in test modes 2 and 3. When exiting the test mode, hardware reset or software reset through writing register 0x0 bit[15] must be performed to ensure normal operation. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 110, 111 = Reserved normal operation.
12	Master/Slave Manual configuration Enable	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11]

				• Link goes down 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration.
11	Master/Slave configuration	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down This bit is ignored if bit[12] is 0. 1 = Manual configuration as MASTER 0 = Manual configuration as SLAVE.
10	Port Type	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down This bit is ignored if bit[12] is 1. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
9	1000BASE-T Full	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
8	1000BASE-T Half-	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised (default)
7:0	Reserved	RW	0x0	Write as 0, ignore on read.

6.2.11. MASTER-SLAVE Status Register (0x0A)

Table 30. MASTER-SLAVE Status Register (0x0A)

Bit	Symbol	Access	Default	Description
15	Master/Slave_cfg_error	RO RC SWC LH	0x0	This register bit will clear on read, rising of MII 0.12 and rising of AN complete. 1 = Master/Slave configuration fault detected 0 = No fault detected
14	Master/Slave	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Local PHY configuration resolved to Master 0 = Local PHY configuration resolved to Slave
13	Local Receiver Status	RO	0x0	1 = Local Receiver OK 0 = Local Receiver not OK
12	Remote Receiver	RO	0x0	1 = Remote Receiver OK 0 = Remote Receiver not OK
11	Link Partner	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Link Partner supports 1000BASE-T half duplex 0 = Link Partner does not support 1000BASE-T half duplex
10	Link Partner	RO	0x0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Link Partner supports 1000Base-T full duplex 0 = Link Partner does not support 1000Base-T full duplex
9:8	Reserved	RO	0x0	Reserved
7:0	Idle Error Count	RO SC	0x0	MSB of Idle Error Counter. The register indicates the idle error count since the last read operation performed to this register. The counter pegs at 11111111 and does not roll over.

6.2.12. MMD Access Control Register (0x0D)

Table 31. MMD Access Control Register (0x0D)

Bit	Symbol	Access	Default	Description
15:14	Function	RW	0x0	00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only
13:5	Reserved	RO	0x0	Reserved
4:0	DEVAD	RW	0x0	MMD register device address. 00001 = MMD1 00011 = MMD3 00111 = MMD7

6.2.13. MMD Access Data Register (0x0E)

Table 32. MMD Access Data Register (0x0E)

Bit	Symbol	Access	Default	Description
15:0	Address data	RW	0x0	If register 0xD bits [15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register.

6.2.14. Extended status register (0x0F)

Table 33. Extended status register (0x0F)

Bit	Symbol	Access	Default	Description
15	1000BASE-X Full Duplex	RO	0x0	1 = PHY supports 1000BASE-X Full Duplex 0 = PHY does not supports 1000BASE-X Full Duplex Always 0.
14	1000BASE-X Half Duplex	RO	0x0	1 = PHY supports 1000BASE-X Half Duplex. 0 = PHY does not support 1000BASE-X Half Duplex. Always 0
13	1000BASE-T Full Duplex	RO	0x1	1 = PHY supports 1000BASE-T Full Duplex 0 = PHY does not supports 1000BASE-T Full Duplex Always 1
12	1000BASE-T Half Duplex	RO	0x0	1 = PHY supports 1000BASE-T Half Duplex 0 = PHY does not support 1000BASE-T Half Duplex Always 0.
11:0	Reserved	RO	0x0	Reserved

6.2.15. PHY Specific Function Control Register (0x10)

Table 34. PHY Specific Function Control Register (0x10)

Bit	Symbol	Access	Default	Description
15:7	Reserved	RO	0x0	Reserved
6:5	Cross_md	RW	0x3	Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. And the configuration does not take effect until software reset. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Reserved	RO	0x0	Reserved
3	Crs_on_tx	RW	0x0	This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode: 1 = Assert CRS on transmitting or receiving 0 = Never assert CRS on transmitting, only assert it on receiving.
2	En_sqe_test	RW	0x0	1 = SQE test enabled, 0 = SQE test disabled Note: SQE Test is automatically disabled in full-duplex mode regardless the setting in this bit.
1	En_pol_inv	RW	0x1	If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te. 1 = Polarity Reversal Enabled 0 = Polarity Reversal Disabled
0	Dis_jab	RW	0x0	Jabber takes effect only in 10BASE-Te half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function

6.2.16. PHY Specific Status Register (0x11)

Table 35. PHY Specific Status Register (0x11)

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	0x0	These status bits are valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received real-time	RO	0x0	1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	When Auto-Negotiation is disabled, this bit is set to 1 for force speed mode. 1 = Resolved 0 = Not resolved
10	Link status real-time	RO	0x0	1 = Link up 0 = Link down
9:7	Reserved	RO	0x0	Reserved
6	MDI Crossover Status	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. The bit value depends on register 0x10 “PHY specific function control register” bits6~bit5 configurations. Register 0x10 configurations take effect after software reset. 1 = MDIX 0 = MDI
5	Wirespeed downgrade	RO	0x0	1 = Downgrade 0 = No Downgrade
4	Reserved	RO	0x0	Reserved
3	Transmit Pause	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed. This bit indicates MAC pause resolution. This bit is for information purposes only and is not used by the device. When in force mode, this bit is set to be 0. 1 = Transmit pause enabled 0 = Transmit pause disabled
2	Receive Pause	RO	0x0	This status bit is valid only when bit[11] is 1. Bit[11] is set when Auto-Negotiation is completed. This bit indicates MAC pause resolution. This bit is for information purposes only and is not used by the device. When in force mode, this bit is set to be 0. 1 = Receive pause enabled 0 = Receive pause disabled

1	Polarity Real Time	RO	0x0	1 = Reverted polarity 0 = Normal polarity
0	Jabber Real Time	RO	0x0	1 = Jabber 0 = No jabber

6.2.17. Interrupt Mask Register (0x12)

Table 36. Interrupt Mask Register (0x12)

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation Error INT mask	RW	0x0	1 = Interrupt enable 0 = Interrupt disable
14	Speed Changed INT mask	RW	0x0	same as bit 15
13	Duplex changed INT mask	RW	0x0	same as bit 15
12	Page Received INT mask	RW	0x0	same as bit 15
11	Link Failed INT mask	RW	0x0	same as bit 15
10	Link Succeed INT mask	RW	0x0	same as bit 15
9:7	reserved	RW	0x0	No used.
6	WOL INT mask	RW	0x0	same as bit 15
5	Wirespeed downgraded INT mask	RW	0x0	same as bit 15
4	Reserved	RW	0x0	No used.
3	Serdes Link Failed INT mask	RW	0x0	same as bit 15
2	Serdes Link Success INT mask	RW	0x0	same as bit 15
1	Polarity changed INT mask	RW	0x0	same as bit 15
0	Jabber Happened INT mask	RW	0x0	same as bit 15

6.2.18. Interrupt Status Register (0x13)

Table 37. Interrupt Status Register (0x13)

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation Error INT	RW	0x0	Error can take place when any of the following happens: • MASTER/SLAVE does not resolve correctly • Parallel detect fault • No common HCD • Link does not come up after negotiation is complete • Selector Field is not equal • flp_receive_idle=true while Autoneg Arbitration FSM is in NEXT PAGE WAIT state 1 = Auto-Negotiation Error takes place 0 = No Auto-Negotiation Error takes place
14	Speed Changed INT	RW	0x0	1 = Speed changed 0 = Speed not changed
13	Duplex changed INT	RW	0x0	1 = duplex changed 0 = duplex not changed
12	Page Received INT	RW	0x0	1 = Page received 0 = Page not received
11	Link Failed INT	RW	0x0	1 = Phy link down takes place

				0 = No link down takes place
10	Link Succeed INT	RW	0x0	1 = Phy link up takes place 0 = No link up takes place
6	WOL INT	RW	0x0	Reserved
5	Wirespeed downgraded INT	RW	0x0	1 = PHY received WOL magic frame. 0 = PHY didn't receive WOL magic frame
4	Reserved	RW	0x0	1 = speed downgraded. 0 = Speed didn't downgrade.
3	Serdes Link Failed INT	RW	0x0	Reserved
2	Serdes Link Success INT	RW	0x0	1 = Sds link down takes place 0 = No Sds link down takes place
1	Polarity changed INT	RW	0x0	1 = Sds link up takes place 0 = No Sds link up takes place
0	Jabber Happened INT	RW	0x0	1 = PHY revered MDI polarity 0 = PHY didn't revert MDI polarity

6.2.19. Speed Auto Downgrade Control Register (0x14)

Table 38. Speed Auto Downgrade Control Register (0x14)

Bit	Symbol	Access	Default	Description
15:6	Reserved	RO	0x0	Reserved
5	En_speed_downgrade	RW	0x0	When this bit is set to 1, the PHY enables smart-speed function. Writing this bit requires a software reset to update.
4:2	Autoneg retry limit pre-downgrade	RW	0x3	If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits.
1:0	Reserved	RO	0x0	Reserved

6.2.20. Rx Error Counter Register (0x15)

Table 39. Rx Error Counter Register (0x15)

Bit	Symbol	Access	Default	Description
15:0	Rx_err_counter	RO	0x0	This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16'hFFFF and not roll over.

6.2.21. Extended Register's Address Offset Register (0x1E)

Table 40. Extended Register's Address Offset Register (0x1E)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved
7:0	Extended Register Address Offset	RW	0x0	It's the address offset of the extended register that will be Write or Read

6.2.22. Extended Register's Data Register (0x1F)

Table 41. Extended Register's Data Register (0x1F)

Bit	Symbol	Access	Default	Description
15:0	Extended Register Data	RW	0x0	It's the data to be written to the extended register

				indicated by the address offset in register 0x1E, or the data read out from that extended register.

6.3. Phy EXT Register

6.3.1. Pkgen Cfg1 (EXT_0x38)

Table 42. Pkgen Cfg1 (EXT_0x38)

Bit	Symbol	Access	default	Description
15:13	Reserved	RW	0x0	Reserved
12	En_pkgen_da_sa	RW	0x0	
11	Pkgen_brdcst	RW	0x0	
10	Pkgchk_txsrc_sel	RW	0x0	1'b1: package check will check tx data after pkgen; 1'b0: package checkc will check tx data before pkgen
9	Pkgen_en_az	RW	0x0	
8:0	Pkgen_in_az_t	RW	0x1ff	

6.3.2. Pkgen Cfg3 (EXT_0x3A)

Table 43. Pkgen Cfg3 (EXT_0x3A)

Bit	Symbol	Access	default	Description
7:0	Pkgen_da	RW	0x0	lowest 8 bits of mac destination address, others is zero
7:0	Pkgen_sa	RW	0x0	lowest 8 bits of mac source address, others is zero

6.3.3. Pkg Cfg0 (EXT_0xA0)

Table 44. Pkg Cfg0 (EXT_0xA0)

Bit	Symbol	Access	default	Description
15	Pkg_chk_en	RW	0x0	1: to enable RX/TX package checker. RX checker checks the MII data at transceiver's PCS RX; TX checker checks the MII data at mii_bridge's TX.
14	Pkg_en_gate	RW	0x1	1: to enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0; 0: not gate the clocks.
13	Bp_pkg_gen	RW	0x1	1: normal mode, to send xMII TX data from PAD; 0: test mode, to send out the MII data generated by pkg_gen module.
12	Pkg_gen_en	RW SC	0x0	1: to enable pkg_gen generating MII packages. But, the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0. If pkg_burst_size is 0, continuous packages will be generated and will be stopped only when pkg_gen_en is set to 0; Otherwise, after the expected packages are generated, pkg_gen will stop, pkg_gen_en will be self-cleared.
11:8	Pkg_prm_lth	RW	0x8	The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will

				be ignored by the pkg_gen module.
7:4	Pkg_ipg_lth	RW	0xd	The IPG of the generated packages, in Byte unit for setting smaller than 12. For setting 13, ipg is 2ms; for setting 14, ipg is 20ms; for 15, ipg is 400ms; Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
3	Xmit_mac_force_gen	RW	0x0	1: To enable pkg_gen to send out the generated data even when the link is not established.
2	Pkg_corrupt_crc	RW	0x0	1: to make pkg_gen to send out CRC error packages. 0: pkg_gen sends out CRC good packages.
1:0	Pkg_payload	RW	0x0	Control the payload of the generated packages. 00: increased Byte payload; 01: random payload; 10: fix pattern 0x5AA55AA5... 11: reserved.

6.3.4. Pkg Cfg1 (EXT_0xA1)

Table 45. Pkg Cfg1 (EXT_0xA1)

Bit	Symbol	Access	default	Description
15:0	Pkg_length	RW	0x40	To set the length of the generated packages.

6.3.5. Pkg Cfg2 (EXT_0xA2)

Table 46. Pkg Cfg2 (EXT_0xA2)

Bit	Symbol	Access	default	Description
15:0	Pkg_burst_size	RW	0x0	To set the number of packages in a burst of package generation.

6.3.6. Pkg Rx Valid0 (Ext_0xA3)

Table 47. Pkg Rx Valid0 (Ext_0xA3)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_valid_high	RO RC	0x0	Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

6.3.7. Pkg Rx Valid1 (Ext_0xA4)

Table 48. Pkg Rx Valid1 (Ext_0xA4)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_valid_low	RO RC	0x0	Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

6.3.8. Pkg Rx Os0 (Ext_0xA5)

Table 49. Pkg Rx Os0 (Ext_0xA5)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_good_high	RO RC	0x0	Pkg_ib_os_good[31:16], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.3.9. Pkg Rx Os1 (Ext_0xA6)

Table 50. Pkg Rx Os1 (Ext_0xA6)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_good_low	RO RC	0x0	Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.3.10. Pkg Rx Us0 (Ext_0xA7)

Table 51. Pkg Rx Us0 (Ext_0xA7)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_us_good_high	RO RC	0x0	Pkg_ib_us_good[31:16], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte.

6.3.11. Pkg Rx Us1 (Ext_0xA8)

Table 52. Pkg Rx Us1 (Ext_0xA8)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_us_good_low	RO RC	0x0	Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.3.12. Pkg Rx Err (Ext_0xA9)

Table 53. Pkg Rx Err (Ext_0xA9)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_err	RO RC	0x0	pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518Byte.

6.3.13. Pkg Rx Os Bad (Ext_0xAA)

Table 54. Pkg Rx Os Bad (Ext_0xAA)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_bad	RO RC	0x0	pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >=1518Byte.

6.3.14. Pkg Rx Fragment (Ext_0xAB)

Table 55. Pkg Rx Fragment (Ext_0xAB)

Bit	Symbol	Access	default	Description

15:0	Pkg_ib_frag	RO RC	0x0	pkg_ib_frag is the number of RX packages from wire whose length are <64Byte.

6.3.15. Pkg Rx Nosfd (Ext_0xAC)

Table 56. Pkg Rx Nosfd (Ext_0xAC)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_nosfd	RO/RC	0x0	pkg_ib_nosfd is the number of RX packages from wire whose SFD is missed.

6.3.16. Pkg Tx Valid0 (Ext_0xAD)

Table 57. Pkg Tx Valid0 (Ext_0xAD)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_valid_high	RO RC	0x0	Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

6.3.17. Pkg Tx Valid1 (Ext_0xAE)

Table 58. Pkg Tx Valid1 (Ext_0xAE)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_valid_low	RO/RC	0x0	Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

6.3.18. Pkg Tx Os0 (Ext_0xAF)

Table 59. Pkg Tx Os0 (Ext_0xAF)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_good_high	RO RC	0x0	Pkg_ob_os_good[31:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.3.19. Pkg Tx Os1 (Ext_0xB0)

Table 60. Pkg Tx Os1 (Ext_0xB0)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_good_low	RO RC	0x0	Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.3.20. Pkg Tx Us0 (Ext_0xB1)

Table 61. Pkg Tx Us0 (Ext_0xB1)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_us_good_high	RO RC	0x0	Pkg_ob_us_good[31:0], pkg_ob_us_good is the number of TX packages from MII whose

				CRC are good and length are <64Byte.

6.3.21. Pkg Tx Us1 (Ext_0xB2)

Table 62. Pkg Tx Us1 (Ext_0xB2)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_us_good_low	RO/RC	0x0	Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.3.22. Pkg Tx Err (Ext_0xB3)

Table 63. Pkg Tx Err (Ext_0xB3)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_err	RO RC	0x0	pkg_ob_err is the number of TX packages from MII whose CRC are wrong and length are >=64Byte, <=1518Byte.

6.3.23. Pkg Tx Os Bad (Ext_0xB4)

Table 64. Pkg Tx Os Bad (Ext_0xB4)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_bad	RO RC	0x0	pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length are >=1518Byte.

6.3.24. Pkg Tx Fragment (Ext_0xB5)

Table 65. Pkg Tx Fragment (Ext_0xB5)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_frag	RO RC	0x0	pkg_ob_frag is the number of TX packages from MII whose length are <64Byte.

6.3.25. Pkg Tx Nosfd (Ext_0xB6)

Table 66. Pkg Tx Nosfd (Ext_0xB6)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_nosfd	RO RC	0x0	pkg_ob_nosfd is the number of TX packages from MII whose SFD is missed.

6.4. SDS MII Register

6.4.1. Basic Control Register (0x00)

Table 67. Basic Control Register (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 0: Normal operation 1: PHY reset
14	Loopback	RW SWC	0x0	Internal loopback control 1'b0: disable loopback 1'b1: enable loopback
13	Speed_Selection(LSB)	RW	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero. Bit6 bit13 1 1 = Reserved 1 0 = 1000Mb/s 0 1 = 100Mb/s 0 0 = 10Mb/s
12	Autoneg_En	RW	0x1	1: to enable auto-negotiation;
11	Power_down	RW SWC	0x0	1 = Power down
10	Isolate	RW SWC	0x0	Isolate phy from RGMII/SGMII/FIBER.
9	Re_Autoneg	RW SWS SC	0x0	Auto-Negotiation automatically restarts after hardware or software reset regardelss of bit[9] RESTART.
8	Duplex_Mode	RW	0x1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0. 1 = Full Duplex 0 = Half Duplex
7	Collision_Test	RW SWC	0x0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted.
6	Speed_ Selection(MSB)	RW	0x1	See bit13.
5:0	Reserved	RW	0x0	Reserved. Write as 0, ignore on read

6.4.2. Basic Status Register (0x01)

Table 68. Basic Status Register (0x01)

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	0x0	PHY doesn't support 100BASE-T4
14	100Base-X_Fd	RO	0x0	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	0x0	PHY supports 100BASE-X_HD

12	10Mbps_Fd	RO	0x0	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	0x0	PHY supports 10Mbps_Hd
10	100Base-T2_Fd	RO	0x0	PHY doesn't support 100Base-T2_Fd
9	100Base-T2_Hd	RO	0x0	PHY doesn't support 100Base-T2_Hd
8	Extended_Status	RO	0x0	Whether support EXTended status register in 0Fh
7	Unidirect_Ability	RO	0x0	1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	0x1	1'b0: PHY will not accept management frames with preamble suppressed
5	Autoneg_Complete	RO SWC	0x0	1'b0: Auto-negotiation process not completed
4	Remote_Fault	RO RC SWC L	0x0	1'b0: no remote fault condition detected
3	Autoneg_Ability	RO	0x1	1'b0: PHY not able to perform Auto-negotiation
2	Link_Status	RO LL SWC	0x0	Link status
1	Jabber_Detect	RO	0x0	always 0
0	Extended_Capability	RO	0x1	To indicate whether support EXTended registers, to access from address register 1Eh and data register 1Fh

6.4.3. Sds Identification Register1 (0x02)

Table 69. Sds Identification Register1 (0x02)

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	0x0	Bits 3 to 18 of the Organizationally Unique Identifier

6.4.4. Sds Identification Register2 (0x03)

Table 70. Sds Identification Register2 (0x03)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	0x0	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0x11	6 bits manufacturer's type number
3:0	Revision_No	RO	0xa	4 bits manufacturer's revision number

6.4.5. Auto-Negotiation Advertisement (0x04)

Table 71. Auto-Negotiation Advertisement (0x04)

Bit	Symbol	Access	Default	Description
15	NEXT_Page	RW	0x0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
14	Ack	RO	0x0	Always 0
13:12	Remote_Fault	RO	0x0	Always 0
11:9	Reserved	RO	0x0	Reserved
8	Asymmetric_Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration

				does not take effect until any of the following occurs:
7	Pause	RW	0x1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs:
6	Half_duplex	RW	0x0	Half duplex ability
5	Full_duplex	RW	0x1	Full duplex ability
4:0	Reserved	RO	0x0	Reserved

6.4.6. Auto-Negotiation Link Partner Ability (0x05)

Table 72. Auto-Negotiation Link Partner Ability (0x05)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RO SWC	0x0	NEXT page. Received Code Word Bit 15
14	ACK	RO SWC	0x0	Acknowledge. Received Code Word Bit 14
13:12	REMOTE_FAULT	RO SWC	0x0	Remote Fault. Received Code Word Bit 13:12
11:9	RESERVED	RO	0x0	Reserved. Received Code Word Bit 11:9
8:7	PAUSE	RO SWC	0x0	Pause. Received Code Word Bit 8:7
6	HALF_DUPLEX	RO SWC	0x0	Half duplex. Received Code Word Bit 6
5	FULL_DUPLEX	RO SWC	0x0	Full duplex. Received Code Word Bit 5
4:0	RESERVED	RO	0x0	Reserved. Received Code Word Bit 4:0

6.4.7. Auto-Negotiation Expansion Register (0x06)

Table 73. 6.2.7. Auto-Negotiation Expansion Register (0x06)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	Local NEXT Page able	RO	0x0	1 = Local Device supports NEXT Page
1	Page received	RO RC LH	0x0	1 = A new page is received
0	Reserved	RO	0x0	Reserved

6.4.8. Auto-Negotiation NEXT Page Register (0x07)

Table 74. Auto-Negotiation NEXT Page Register (0x07)

Bit	Symbol	Access	Default	Description
15:0	NEXT Page	RO	0x0	always be 0

6.4.9. Auto-Negotiation Link Partner Received NEXT Page Register (0x08)

Table 75. Auto-Negotiation Link Partner Received NEXT Page Register (0x08)

Bit	Symbol	Access	Default	Description
15:0	Link Partner NEXT Page	RO	0x0	always be 0

6.4.10. Extended status register (0x0F)

Table 76. Extended status register (0x0F)

Bit	Symbol	Access	Default	Description
15	1000BASE-X Full Duplex	RO	0x1	1 = PHY supports 1000BASE-X Full Duplex

14	1000BASE-X Half Duplex	RO	0x0	1 = PHY supports 1000BASE-X Half Duplex.
13	1000BASE-T Full Duplex	RO	0x0	1 = PHY supports 1000BASE-T Full Duplex
12	1000BASE-T Half Duplex	RO	0x0	1 = PHY supports 1000BASE-T Half Duplex
11:0	Reserved	RO	0x0	Always 0

6.4.11. Sds Specific Status Register (0x11)

Table 77. Sds Specific Status Register (0x11)

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	0x0	These status bits are valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.
13	Duplex	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.
12:11	Pause	RO	0x0	Pause to mac
10	Link status real-time	RO	0x0	1 = Link up
9	Rx_lpi_active	RO	0x0	rx lpi is active
8	Duplex_error	RO	0x0	realtime duplex error
7	En_flowctrl_rx	RO	0x0	realtime en_flowctrl_rx
6	En_flowctrl_tx	RO	0x0	realtime en_flowctrl_tx
5:4	Ser_mode_cfg	RO	0x0	realtime serdes working mode
3:1	Xmit	RO	0x0	realtime transmit statemachine
0	Syncstatus	RO	0x0	realtime syncstatus

6.4.12. 100FX Cfg (0x14)

Table 78. 100FX Cfg (0x14)

Bit	Symbol	Access	Default	Description
15	Force_sg_status	RW	0x0	Force sds linkup
14	Duplex_to_mac_100fx	RW	0x1	duplex setting to mac in 100fx mode
13:12	Pause_to_mac_100fx	RO	0x3	Pause setting to mac in 100fx mode
11:0	Reserved	RO	0x0	Reserved

6.4.13. Receive Err Counter (0x15)

Table 79. Receive Err Counter (0x15)

Bit	Symbol	Access	Default	Description
15:0	error_counter_rx	RO	0x0	receive error counter

6.4.14. Link Fail Counter (0x16)

Table 80. Link Fail Counter (0x16)

Bit	Symbol	Access	Default	Description
15:8	Reserved	RO	0x0	Reserved
7:0	Link_fail_cnt	RO	0x0	link fail counter

6.5. SDS ext Register

6.5.1. Pkgen Cfg1 (EXT_0x38)

Table 81. Pkgen Cfg1 (EXT_0x38)

Bit	Symbol	Access	default	Description
15:13	Reserved	RW	0x0	Reserved
12	En_pkgen_da_sa	RW	0x0	
11	Pkgen_brdcst	RW	0x0	
10	Pkgchk_txsrc_sel	RW	0x0	
9	Pkgen_en_az	RW	0x0	
8:0	Pkgen_in_az_t	RW	0x1ff	

6.5.2. Pkgen Cfg3 (EXT_0x3A)

Table 82. Pkgen Cfg3 (EXT_0x3A)

Bit	Symbol	Access	Default	Description
7:0	Pkgen_da	RW	0x0	
7:0	Pkgen_sa	RW	0x0	

6.5.3. Pkg Cfg0 (EXT_0x1A0)

Table 83. Pkg Cfg0 (EXT_0x1A0)

Bit	Symbol	Access	default	Description
15	Pkg_chk_en	RW	0x0	1: to enable RX/TX package checker. RX checker checks the MII data at transceiver's PCS RX; TX checker checks the MII data at mii_bridge's TX.
14	Pkg_en_gate	RW	0x1	1: to enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0;
13	Bp_pkg_gen	RW	0x1	1: normal mode, to send xMII TX data from PAD;
12	Pkg_gen_en	RW SC	0x0	1: to enable pkg_gen generating MII packages. But, the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0.
11:8	Pkg_prm_lth	RW	0x8	The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
7:4	Pkg_ipg_lth	RW	0xc	The IPG of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
3	Xmit_mac_force_gen	RW	0x0	1: To enable pkg_gen to send out the generated data even when the link is not established.
2	Pkg_corrupt_crc	RW	0x0	1: to make pkg_gen to send out CRC error packages.
1:0	Pkg_payload	RW	0x0	Control the payload of the generated packages.

6.5.4. Pkg Cfg1 (EXT_0x1A1)

Table 84. Pkg Cfg1 (EXT_0x1A1)

Bit	Symbol	Access	default	Description
15:0	Pkg_length	RW	0x40	To set the length of the generated packages.

6.5.5. Pkg Cfg2 (EXT_0x1A2)

Table 85. Pkg Cfg2 (EXT_0x1A2)

Bit	Symbol	Access	default	Description
15:0	Pkg_burst_size	RW	0x0	To set the number of packages in a burst of package generation.

6.5.6. Pkg Rx Valid0 (Ext_0x1A3)

Table 86. Pkg Rx Valid0 (Ext_0x1A3)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_valid_high	RO RC	0x0	Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

6.5.7. Pkg Rx Valid1 (Ext_0x1A4)

Table 87. Pkg Rx Valid1 (Ext_0x1A4)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_valid_low	RO RC	0x0	Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

6.5.8. Pkg Rx Os0 (Ext_0x1A5)

Table 88. Pkg Rx Os0 (Ext_0x1A5)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_good_high	RO RC	0x0	Pkg_ib_os_good[31:16], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.5.9. Pkg Rx Os1 (Ext_0x1A6)

Table 89. Pkg Rx Os1 (Ext_0x1A6)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_good_low	RO RC	0x0	Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.5.10. Pkg Rx Us0 (Ext_0x1A7)

Table 90. Pkg Rx Us0 (Ext_0x1A7)

Bit	Symbol	Access	default	Description

15:0	Pkg_ib_us_good_high	RO RC	0x0	Pkg_ib_us_good[31:16], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte.

6.5.11. Pkg Rx Us1 (Ext_0x1A8)

Table 91. Pkg Rx Us1 (Ext_0x1A8)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_us_good_low	RO RC	0x0	Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

6.5.12. Pkg Rx Err (Ext_0x1A9)

Table 92. Pkg Rx Err (Ext_0x1A9)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_err	RO RC	0x0	pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518Byte.

6.5.13. Pkg Rx Os Bad (Ext_0x1AA)

Table 93. Pkg Rx Os Bad (Ext_0x1AA)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_bad	RO RC	0x0	pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >=1518Byte.

6.5.14. Pkg Rx Fragment (Ext_0x1AB)

Table 94. Pkg Rx Fragment (Ext_0x1AB)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_frag	RO RC	0x0	pkg_ib_frag is the number of RX packages from wire whose length are <64Byte.

6.5.15. Pkg Rx Nosfd (Ext_0x1AC)

Table 95. Pkg Rx Nosfd (Ext_0x1AC)

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_nosfd	RO/RC	0x0	pkg_ib_nosfd is the number of RX packages from wire whose SFD is missed.

6.5.16. Pkg Tx Valid0 (Ext_0x1AD)

Table 96. Pkg Tx Valid0 (Ext_0x1AD)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_valid_high	RO RC	0x0	Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and

				<=1518Byte.

6.5.17. Pkg Tx Valid1 (Ext_0x1AE)

Table 97. Pkg Tx Valid1 (Ext_0x1AE)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_valid_low	RO/RC	0x0	Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

6.5.18. Pkg Tx Os0 (Ext_0x1AF)

Table 98. Pkg Tx Os0 (Ext_0x1AF)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_good_high	RO RC	0x0	Pkg_ob_os_good[31:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.5.19. Pkg Tx Os1 (Ext_0x1B0)

Table 99. Pkg Tx Os1 (Ext_0x1B0)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_good_low	RO RC	0x0	Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.5.20. Pkg Tx Us0 (Ext_0x1B1)

Table 100. Pkg Tx Us0 (Ext_0x1B1)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_us_good_high	RO RC	0x0	Pkg_ob_us_good[31:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are <64Byte.

6.5.21. Pkg Tx Us1 (Ext_0x1B2)

Table 101. Pkg Tx Us1 (Ext_0x1B2)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_us_good_low	RO/RC	0x0	Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

6.5.22. Pkg Tx Err (Ext_0x1B3)

Table 102. Pkg Tx Err (Ext_0x1B3)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_err	RO RC	0x0	pkg_ob_err is the number of TX packages from MII whose CRC are wrong and length are >=64Byte, <=1518Byte.

6.5.23. Pkg Tx Os Bad (Ext_0x1B4)

Table 103. Pkg Tx Os Bad (Ext_0x1B4)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_bad	RO RC	0x0	pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length are >=1518Byte.

6.5.24. Pkg Tx Fragment (Ext_0x1B5)

Table 104. Pkg Tx Fragment (Ext_0x1B5)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_frag	RO RC	0x0	pkg_ob_frag is the number of TX packages from MII whose length are <64Byte.

6.5.25. Pkg Tx Nosfd (Ext_0x1B6)

Table 105. Pkg Tx Nosfd (Ext_0x1B6)

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_nosfd	RO RC	0x0	pkg_ob_nosfd is the number of TX packages from MII whose SFD is missed.

7. Timing and AC/DC Characteristics

7.1. DC Characteristics

Table 106. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
DVDD33, AVDD33	3.3V Supply Voltage	-	2.97	3.3	3.63	V
2.5V MDIO, MDC, RGMII I/O	2.5V RGMII Supply Voltage	-	2.25	2.5	2.75	V
1.8V MDIO, MDC, RGMII I/O	1.8V RGMII Supply Voltage	-	1.62	1.8	1.98	V
Voh (3.3V)	Minimum High Level Output Voltage	-	2.4	-	3.6	V
Voh (2.5V)	Minimum High Level Output Voltage	-	2	-	2.8	V
Voh (1.8V)	Minimum High Level Output Voltage	-	1.62		2.1	
Vol (3.3V)	Maximum Low Level Output Voltage	-	-0.3	-	0.4	V
Vol (2.5V)	Maximum Low Level Output Voltage	-	-0.3	-	0.4	V
Vol (1.8V)	Maximum Low Level Output Voltage	-	-0.3		0.4	
Vih (3.3V)	Minimum High Level Input Voltage	-	2	-	-	V
Vil (3.3V)	Maximum Low Level Input Voltage	-	-	-	0.8	V
Vih (2.5V)	Minimum High Level Input Voltage	-	1.7	-	-	V
Vil (2.5V)	Maximum Low Level Input Voltage	-	-	-	0.7	V
Vih (1.8V)	Minimum High Level Input Voltage	-	1.2	-	-	V
Vil (1.8V)	Maximum Low Level Input Voltage	-	-	-	0.5	V

7.2. AC Characteristics

7.2.1. SGMII Differential Transmitter Characteristics

Table 107. SGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ± 300ppm
T_X1	Eye Mask	-	-	0.1875	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	200	-	-	mV	-
T_Y2	Eye Mask	-	-	450	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	700	900	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.625	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.35UI
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling Capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

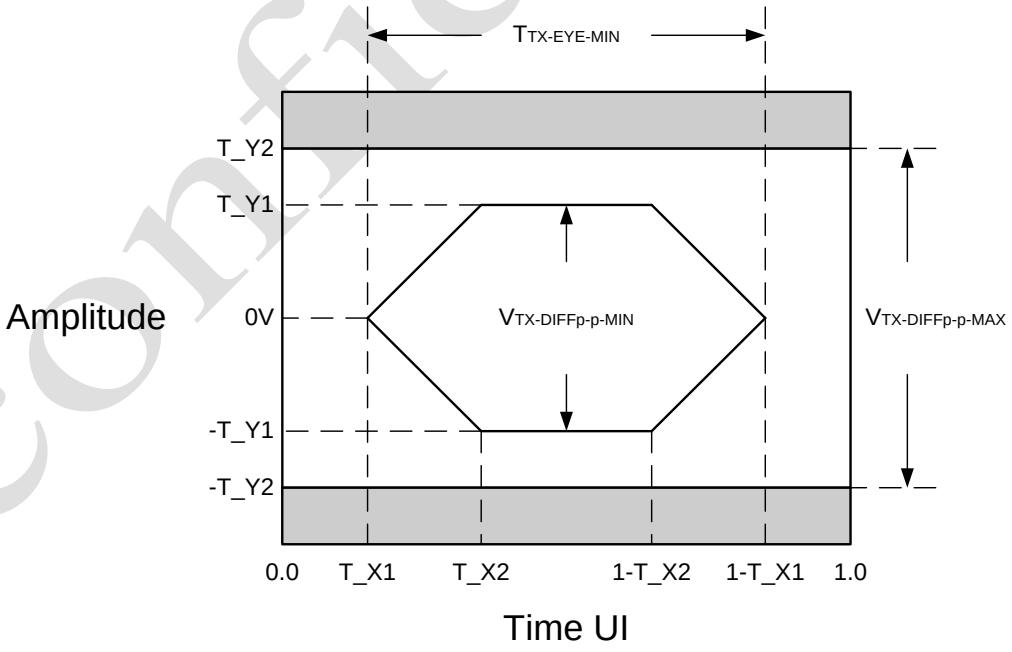


Figure 8. SGMII Differential Transmitter Eye Diagram

7.2.2. SGMII Differential Receiver Characteristics

Table 108. SGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	799.94	800	800.06	ps	800ps ± 300ppm
R_X1	Eye Mask	-	-	0.3125	UI	-
R_Y1	Eye Mask	50	-	-	mV	-
R_Y2	Eye Mask	-	-	600	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	100	-	1200	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.625	UI	$T_{RX-JITTER-MAX}$ = 1 - $T_{RX-EYE-MIN}$ = 0.6UI
R_{RX}	Differential Resistance	80	100	120	ohm	-

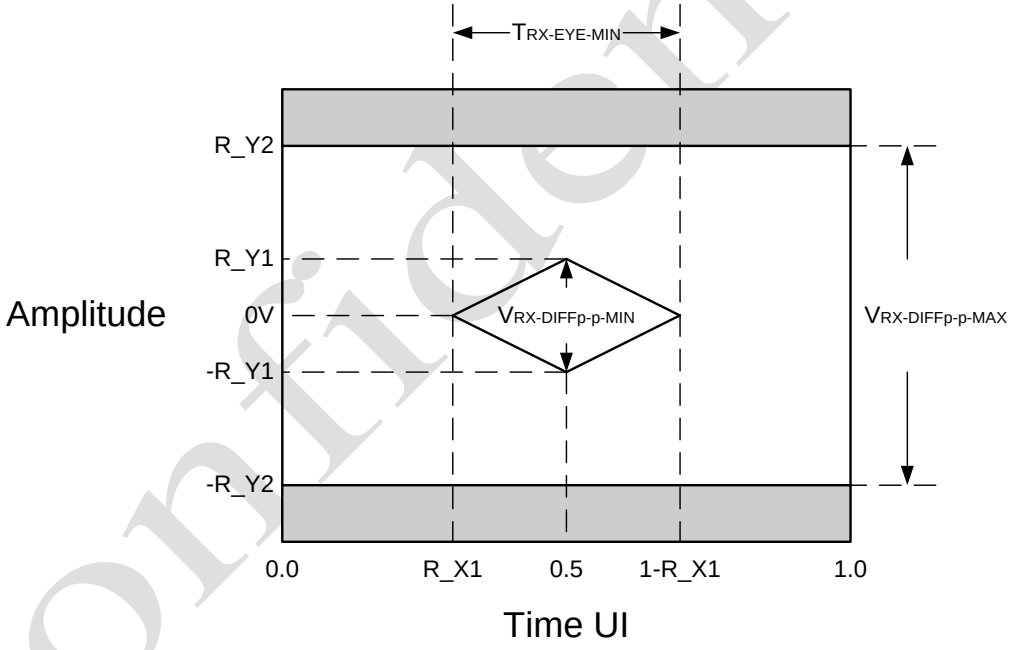


Figure 9. SGMII Differential Receiver Eye Diagram

7.2.3. RGMII Timing w/o delay

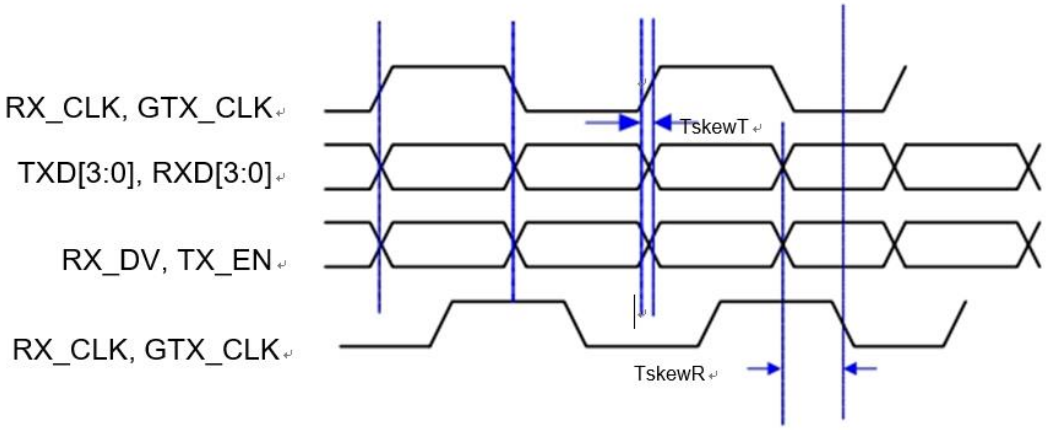


Figure 10. RGMII Timing w/o delay

Table 109. RGMII Timing w/o delay

Symbol	Parameter	Min	Typ	Max	Unit
TskewT	Data to clock output skew (at Transmitter)	-500	0	500	ps
TskewR	Data to clock output skew (at Receiver)	1	—	—	ns
Tcyc	Clock cycle duration	7.2	8.0	8.8	ns
Duty_G	Duty cycle for Gigabit	45	50	55	%
Duty_T	Duty cycle for 10/100T	40	50	60	%
Tr/ Tf	Rise/Fall time (20 - 80%)	—	—	0.75	ns

7.2.4. RGMII Timing with internal delay

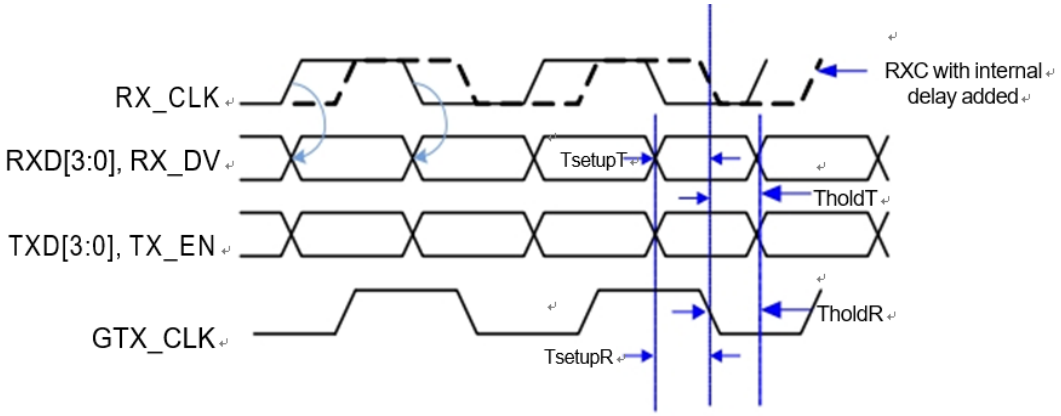


Figure 11. RGMII Timing with internal delay

Table 110. RGMII Timing with internal delay

Symbol	Parameter	Min	Typ	Max	Unit
TsetupT	Data to Clock output Setup (at Transmitter — integrated delay)	1.65	2.0	2.2	ns
TholdT	Clock to Data output Hold (at Transmitter — integrated delay)	1.65	2.0	2.2	ns
TsetupR	Data to Clock input setup Setup (at Receiver — integrated delay)	1.0	2.0		ns
TholdR	Data to Clock output setup Setup (at Reciever — integrated delay)	1.0	2.0		ns

7.2.5. SMI (MDC/MDIO) Interface Characteristics

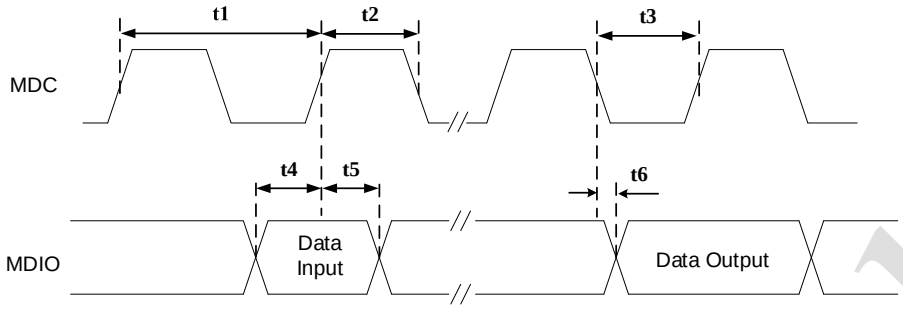


Figure 12. SMI (MDC/MDIO) Timing

Table 111. SMI (MDC/MDIO) Interface Characteristics

Symbol	Description	Min	Typ	Max	Units
t1	MDC Clock Period	-	80	-	ns
t2	MDC High Time	-	32	-	ns
t3	MDC Low Time	-	32	-	ns
t4	MDIO to MDC Rising Setup Time (Data Input)	-	10	-	ns
t5	MDIO to MDC Rising Hold Time (Data Input)	-	10	-	ns
t6	MDIO to MDC Rising Setup Time (Read Data)	0	-	60	ns
t7	MDIO to MDC rising hold time (Read Data)	10	-	-	ns

7.3. Crystal Requirement

Table 112. Crystal Requirement

Symbol	Description	Min	Typ	Max	Unit
F ref	Crystal Reference Frequency	-	25	-	MHz
F ref Tolerance	Crystal Reference Frequency tolerance	-50	-	50	ppm
Duty Cycle	Reference clock input duty cycle	40	-	60	%
ESR	Equivalent Series Resistance	-		50	ohm
DL	Drive Level	-	-	0.5	mW
Vih	Crystal output high level	1.4	-	-	V
Vil	Crystal output low level	-	-	0.4	V

7.4. Oscillator/External Clock Requirement

Table 113. Oscillator/External Clock Requirement

Parameter	Condition	Min	Typ	Max	Unit
Frequency			25		MHz
Frequency tolerance	Ta= -40~85 C	-50		50	PPM
Duty Cycle		40	-	60	%
Peak to Peak Jitter				200	ps
Vih		1.4		AVDD33+0.3	V
Vil				0.4	V
Rise Time	10%~90%			10	ns
Fall Time	10%~90%			10	ns
Temperature Range	YT8521SC	0		70	℃
Temperature Range	YT8521SH	-40		85	℃

8. Power Requirements

8.1. Absolute Maximum Ratings

Table 114. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
VDD33/AVDD33	Supply Voltage 3.3V	-0.3	3.7	V
AVDDL/DVDDL	Supply Voltage 1.2V	-0.2	1.4	V
2.5V RGMII	Supply Voltage 2.5V	-0.3	2.8	V
1.8V RGMII	Supply Voltage 1.8V	-0.3	2.3	V
3.3V DC input	Input Voltage	-0.3	3.6	V
1.2V DC input	Input Voltage	-0.3	1.4	V
Storage Temperature		-55	125	℃

8.2. Recommended Operating Conditions

Table 115. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage	DVDD33, AVDD33	2.97	3.3	3.63	V
	AVDDL, DVDDL	1.14	1.2	1.26	V
	2.5V RGMII	2.25	2.5	2.75	V
	1.8V RGMII	1.62	1.8	1.98	V
YT8521SC Ambient Operating Temperature Ta		0	-	70	℃
YT8521SH Ambient Operating Temperature Ta		-40	-	85	℃
Maximum Junction Temperature				125	℃

8.3. Power Sequence

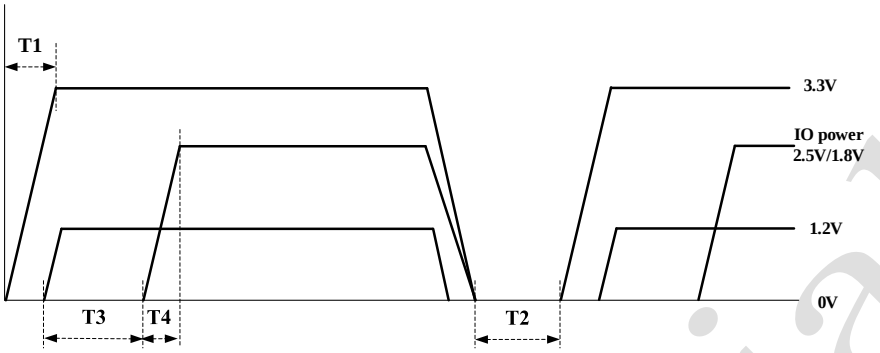


Figure 13. Power Sequence Diagram

Table 116. Power Sequence Timing Parameters

Symbol	Description	Min	Typ	Max	Units
T1	3.3V rising time	0.5	-	-	ms
T2	3.3V and 1.2V power down duration	100	-	-	ms
T3	Core power 1.2V ready time	72	-	-	ms
T4	Internal LDO ready time	1.5	-	-	ms

8.4. Power Noise

The max noise of 3.3V should be under 50mV, and that of 1.2V should be under 30mV.

9. Mechanical and Thermal

9.1. RoHS-Compliant Packaging

Motor-comm offers an RoHS package that is compliant with RoHS

Table 117. Part Number

Part Number	Status	Package	Op temp (℃)	Note
YT8521SC	Active	QFN48 6x6mm	0 to 70	
YT8521SH	Active	QFN48 6x6mm	-40 to 85	

9.2. Thermal Resistance

Table 118. Thermal Resistance

Symbol	Thermal Resistance	Units
θ_{JA}	27.2 (TA =25 °C)	°C/W
	24.3 (TA =100 °C)	°C/W
θ_{JB}	7.1	°C/W
θ_{JC}	17.5	°C/W

Note:

(1) θ_{JA} , Junction-to-ambient thermal resistance

$$\theta_{JA} = (T_J - T_A)/ P_H$$

where θ_{JA} = thermal resistance from junction-to-ambient (°C/W)

T_J = junction temperature when the device has achieved a steady-state after application of P_H (°C)

T_a = ambient temperature (°C)

P_H = power dissipation that produced change in junction temperature (W)

(2) θ_{JB}, junction-to-board thermal resistance

$$\theta_{JB} = (T_J - T_B)/ P_H$$

where θ_{JB}=thermal resistance from junction-to-board as described by this specification(°C/W)

T_J = junction temperature when the device has achieved a steady-state after application of P_H (°C)

T_B = board temperature at steady state(°C)

P_H = power dissipation that produced change in junction temperature (W)

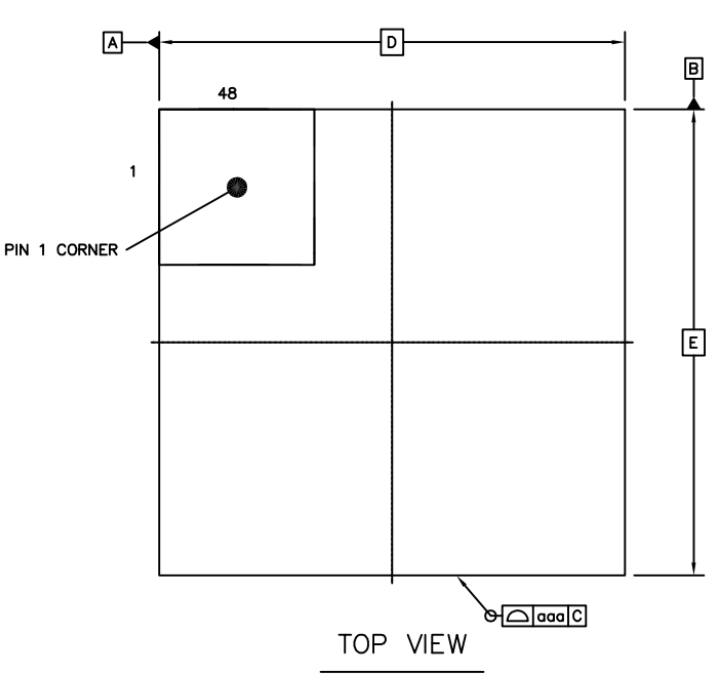
(3) θ_{JC}, junction-to-case thermal resistance

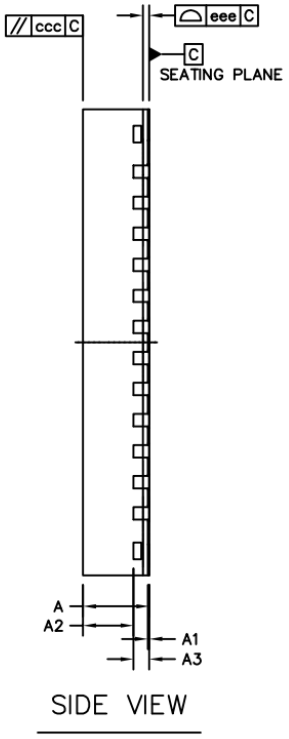
$$\theta_{JC} = (T_J - T_C)/ P_H$$

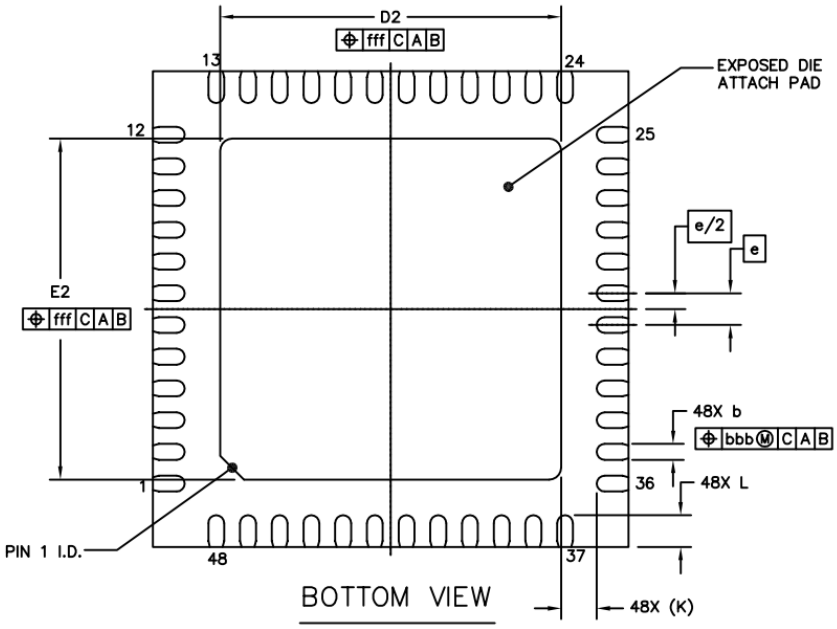
where T_C = case temperature attached with a cold plate

θ_{JC} represents the resistance to the heat flows from the chip to package top case. θJC is important when external heat sink is attached on package top.

10. Mechanical Information







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	4.2	4.3	4.4
	Y	E2	4.2	4.3	4.4
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.45 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

11. Ordering Information

Table 119. Ordering Information

Part Number	Grade	Package	Packaging	Status	Operation Temp
YT8521SC	Consumer	QFN 48 6x6 mm	Tape&Reel Tray	Mass Production	0 ~70°C
YT8521SH	Industrial	QFN 48 6x6 mm	Tape&Reel Tray	Mass Production	-40 ~ 85°C