CEK8903_PIQ_DDR4_ONBOARD

PHYTIUM CONFIDENTIAL

CONTENTS

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CEK8903-PIQ

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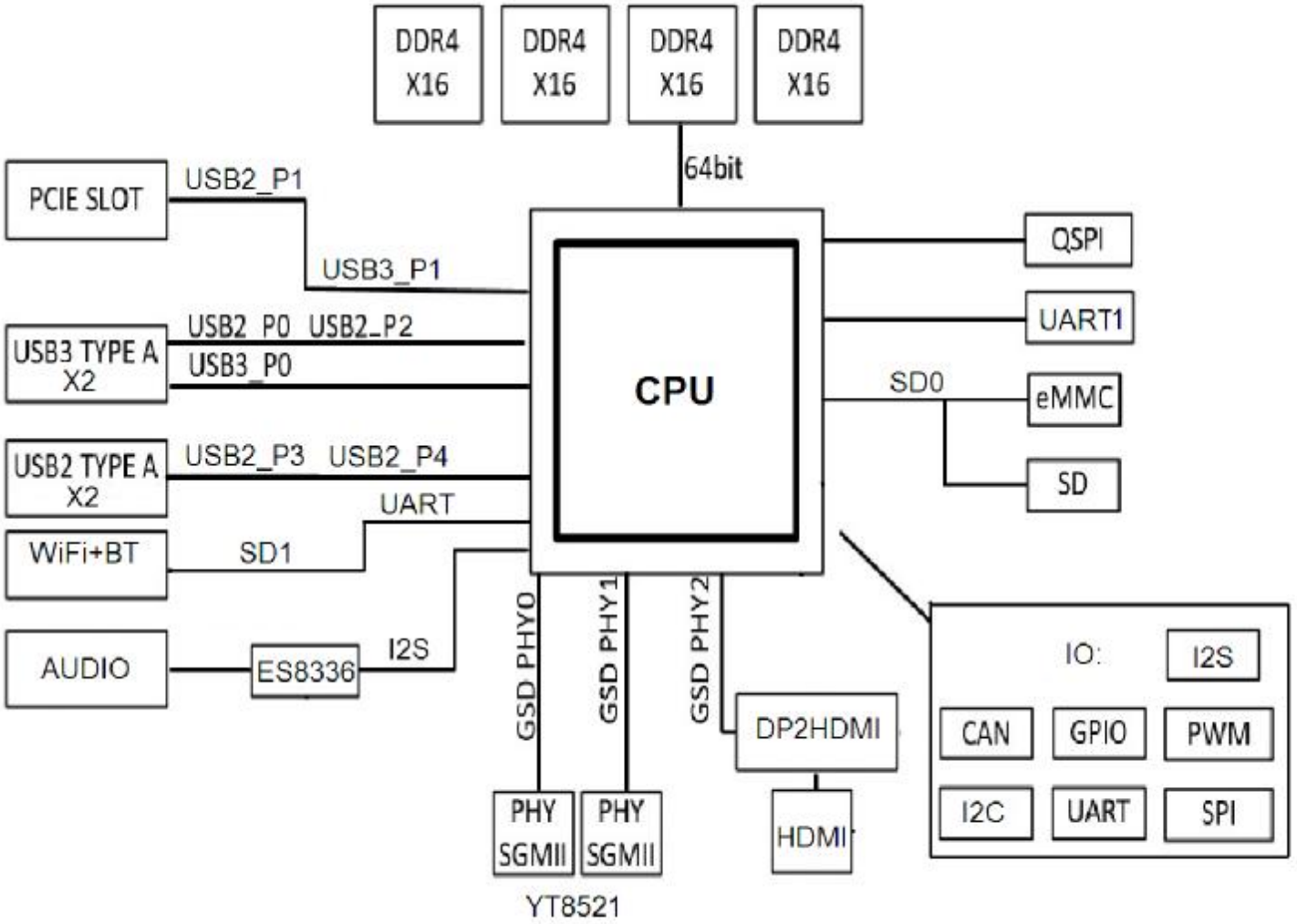

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Title: SYSTEM_BLOCK

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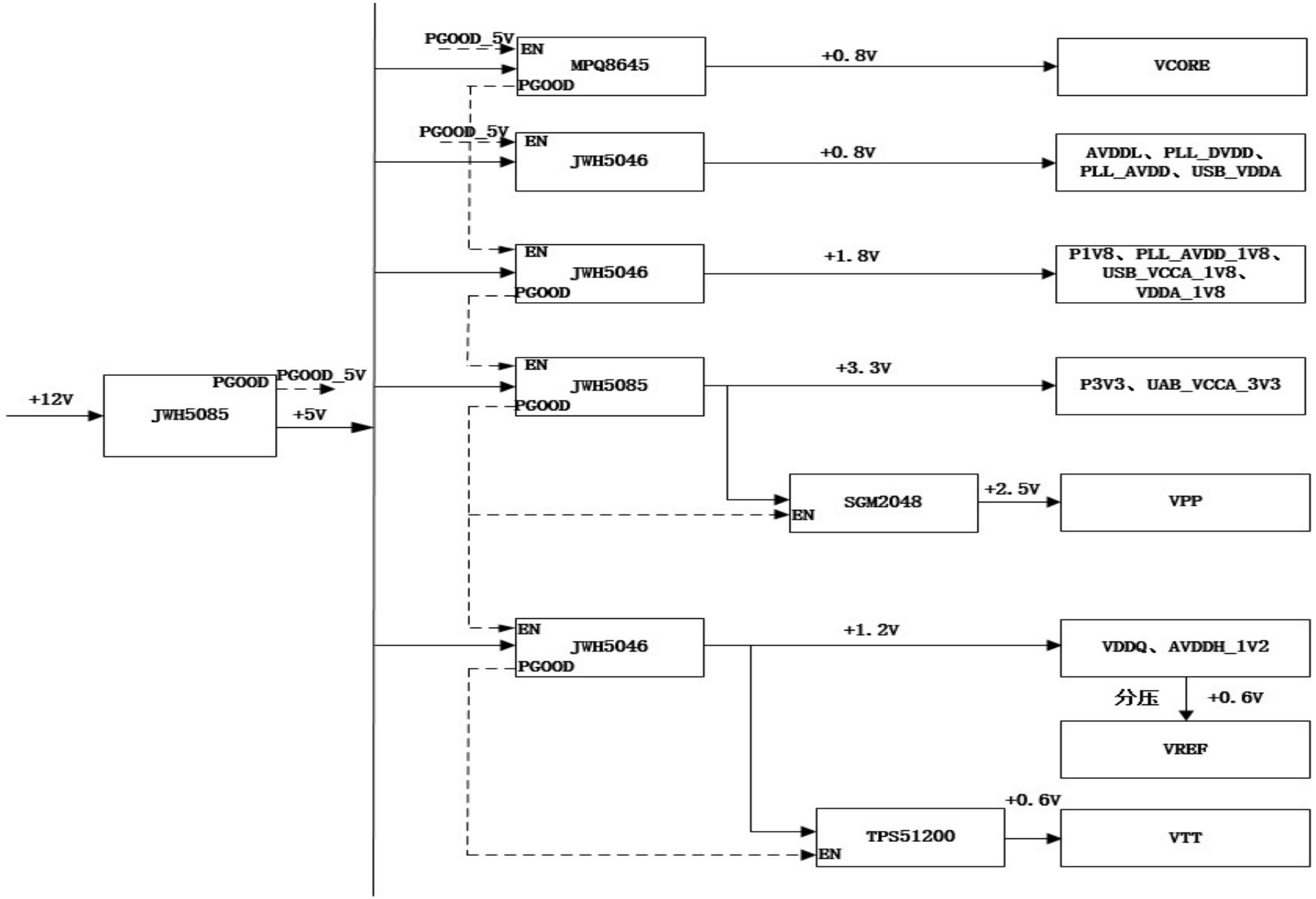

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Title: POWER_BLOCK

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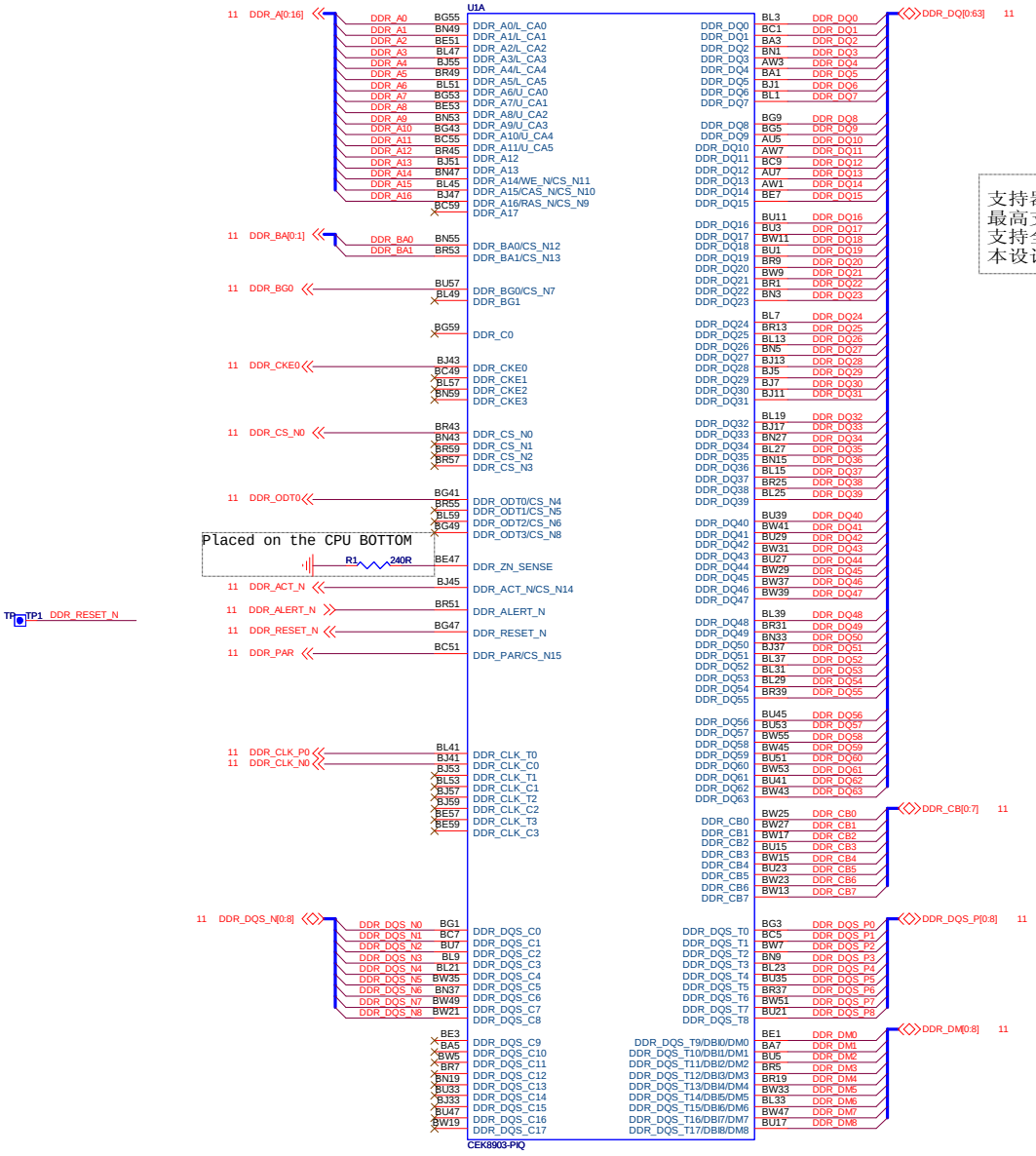

支持器件：DDR4：x4、x8、x16；LPDDR4：x16、x32，
最高支持72个数据位。
支持全位宽模式和半位宽模式（仅支持低32位数据和低4位ECC）
本设计采用DDR4 X16颗粒

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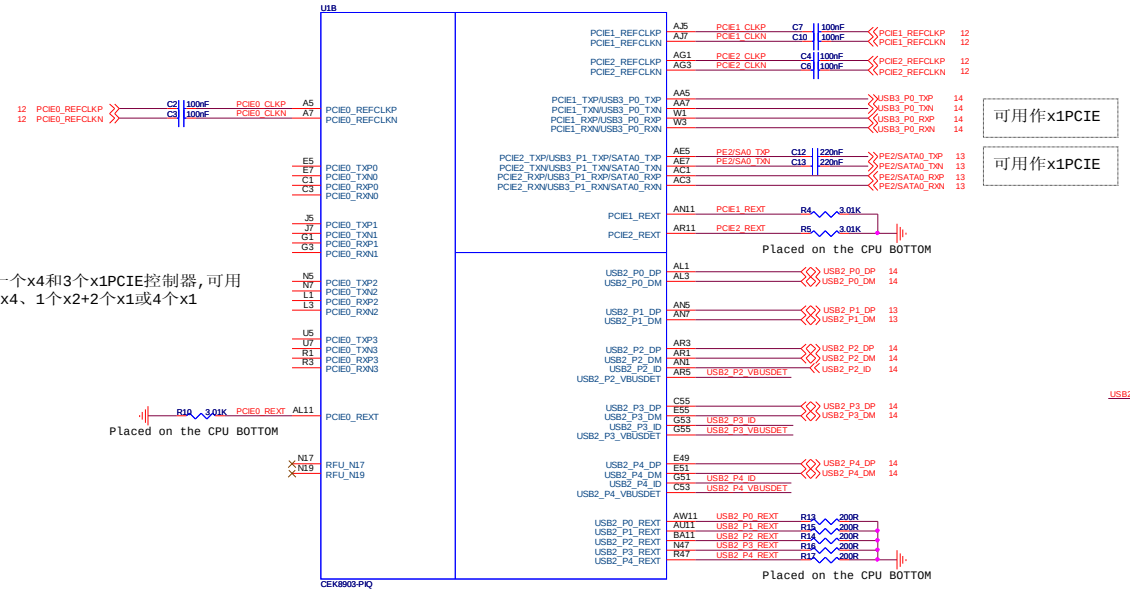
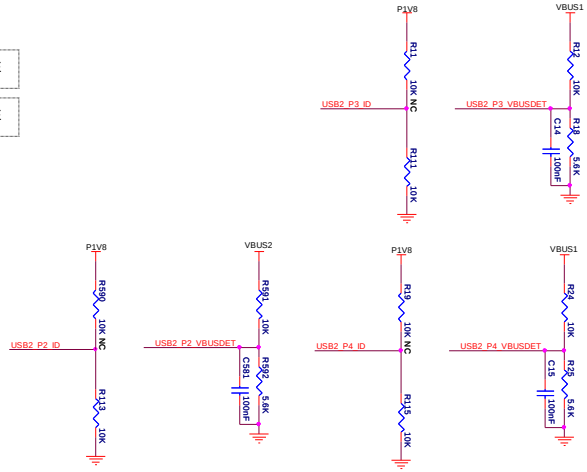
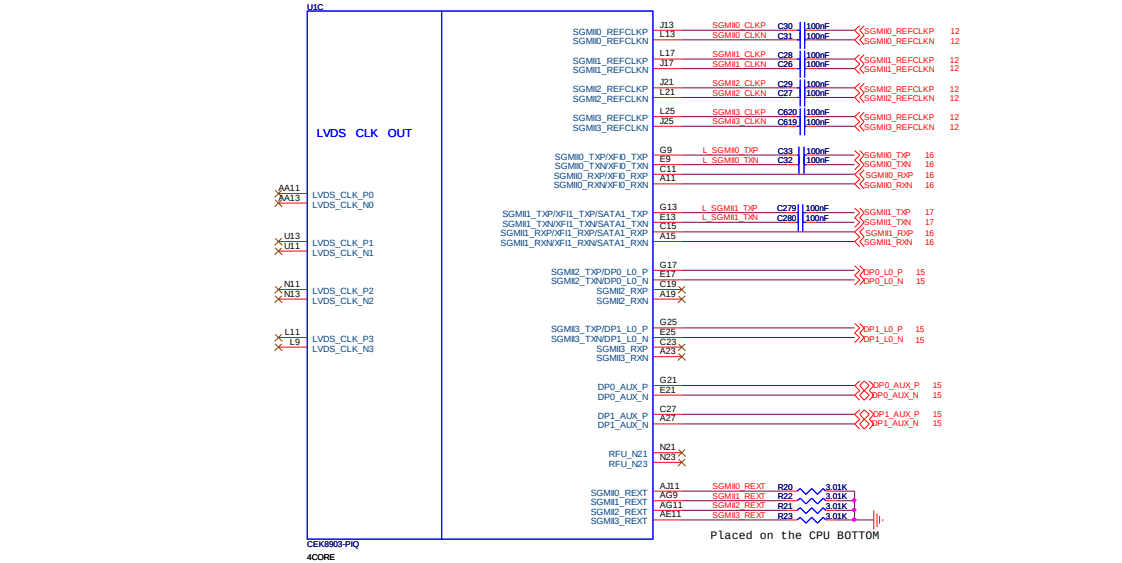


包含一个x4和3个x1PCIE控制器,可用作1个x4、1个x2+2个x1或4个x1

可用作x1PCIE

可用作x1PCIE





CEK8903-PIQ包含了4个MAC控制器MAC0/1支持XFI和SGMII; MAC2/3支持SGMII和RGMII,且共用MDIO。

MDIO管理接口与MAC端口对应关系

MDIO管理接口	MAC端口类型
MDIO0/MDC0	SGMII0
MDIO1/MDC1	SGMII1
MDIO2/MDC2	SGMII2/RGMII0
MDIO3/MDC3	SGMII3/RGMII1

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Title: CPU_SERDES

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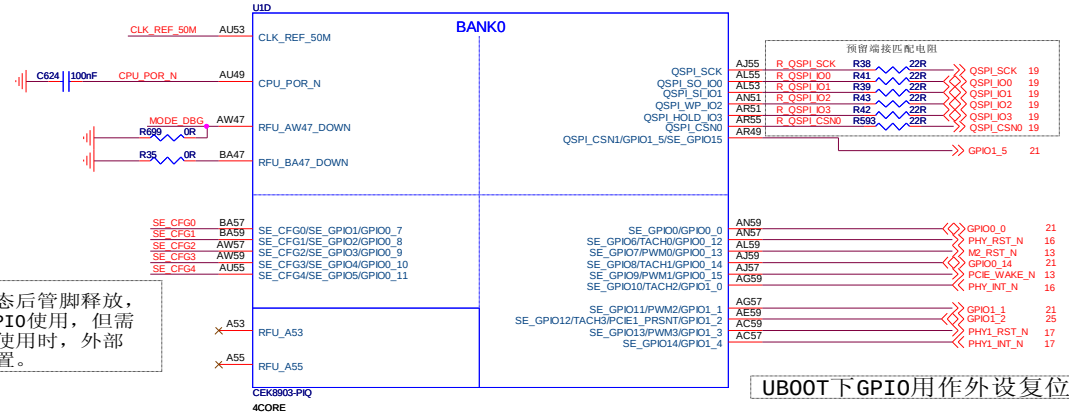
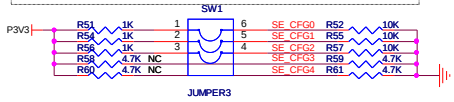


SE_CFG识别到启动设置状态后管脚释放，可以作为通用GPIO与SE_GPIO使用，但需注意这些管脚作为普通IO使用时，外部电气环境不能干扰启动配置。

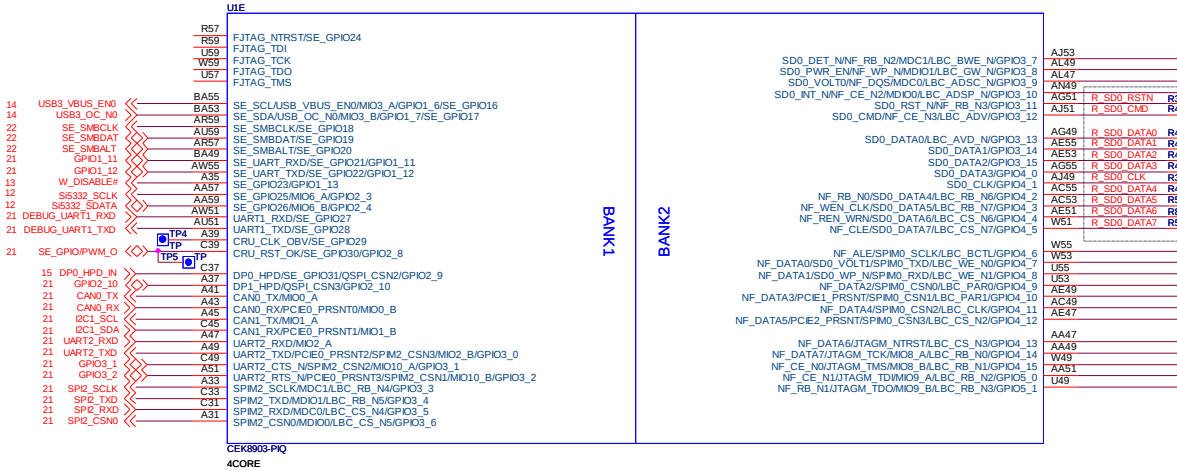
UBOOT下GPIO用作外设复位

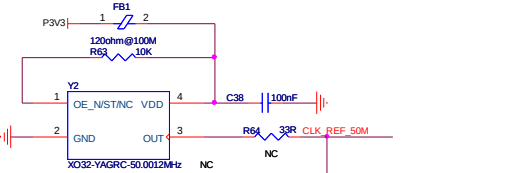
具体应用场景下，建议使用4.7K电阻上下拉确定启动配置信号

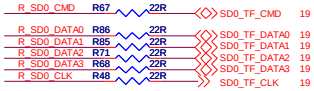


启动配置

SE_CFG[2:0]启动介质:
000:RESERVED
001:QSPI Default
010:LBC
011:NandFlash
100:SD0---SD CARD
101:SD1---SD CARD
110:SD0---eMMC
111:RESERVED
SE_CFG[4:3]启动段位:
00:Default(RECOVER0)
01:RECOVER1
10:RECOVER2
11:RECOVER3







本设计的BANK 电压如下：
bank（0、1、2） ---> 3.3V
bank（3、4、5 ） ---> 1.8V

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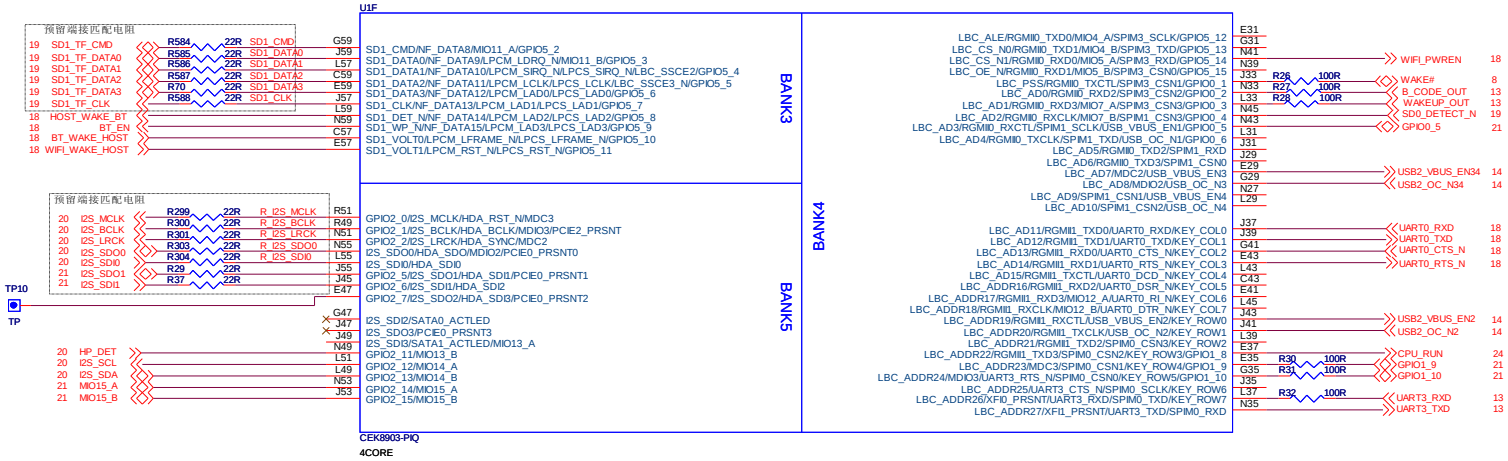

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Title: CPU_GPIO_2

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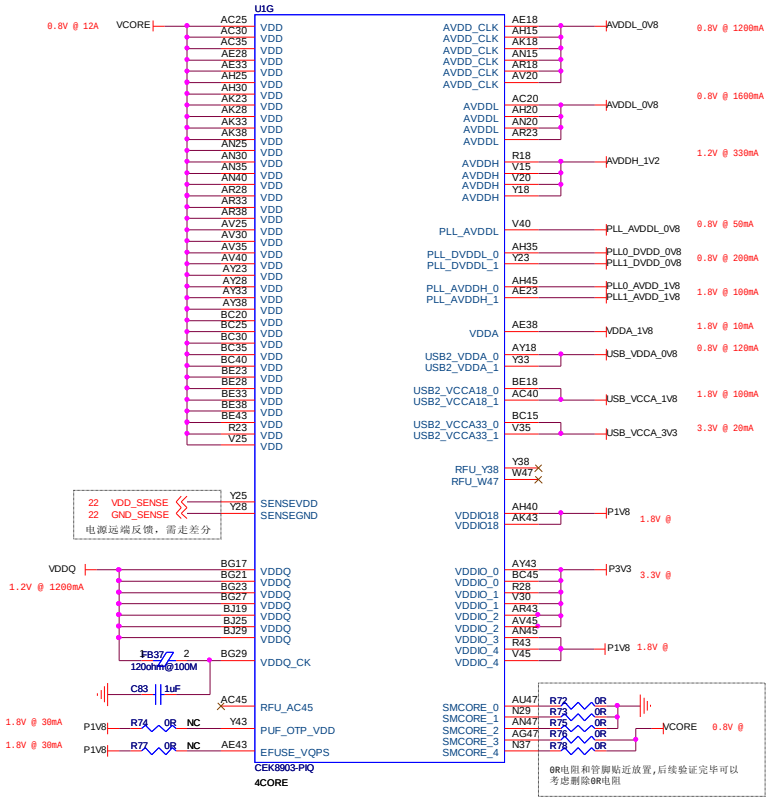

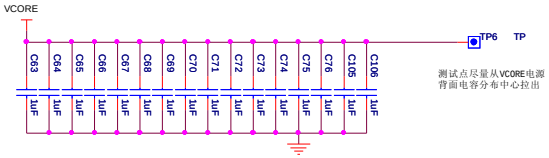

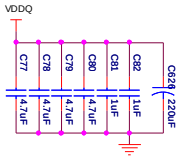

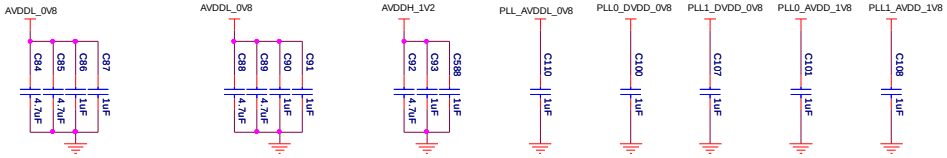

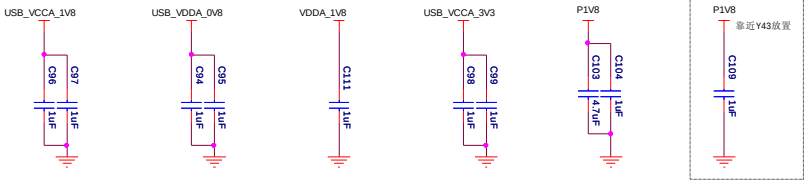

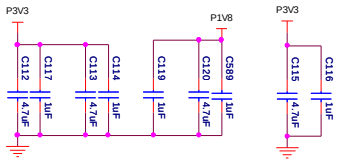

BANK0~BANK4 供电电源为VDDIO_x(0-4),均支持1.8V或3.3V电平;
SMCORE_x(0-4)为各bank电平控制信号，其与VDDIO_x(0-4)对应关系如下表：

SMCORE_x	VDDIO_x
0	3.3V
1	1.8V

1表示SMCORE_x(0-4)接CEK8903-PIQ核心电压VDD
0表示SMCORE_x(0-4)接地

VDDIO18电源为各BANK IO保持电源及BANK5 IO
供电电源，需要保持常供电状态，且固定1.8V。

VDDIO_x接3.3V电源前，SMCORE_x必须接地，上下电过程中须保证
VDDIO_x(3.3V)和VDDIO18的电压压差在1.98V以内,否则有可靠性问题。

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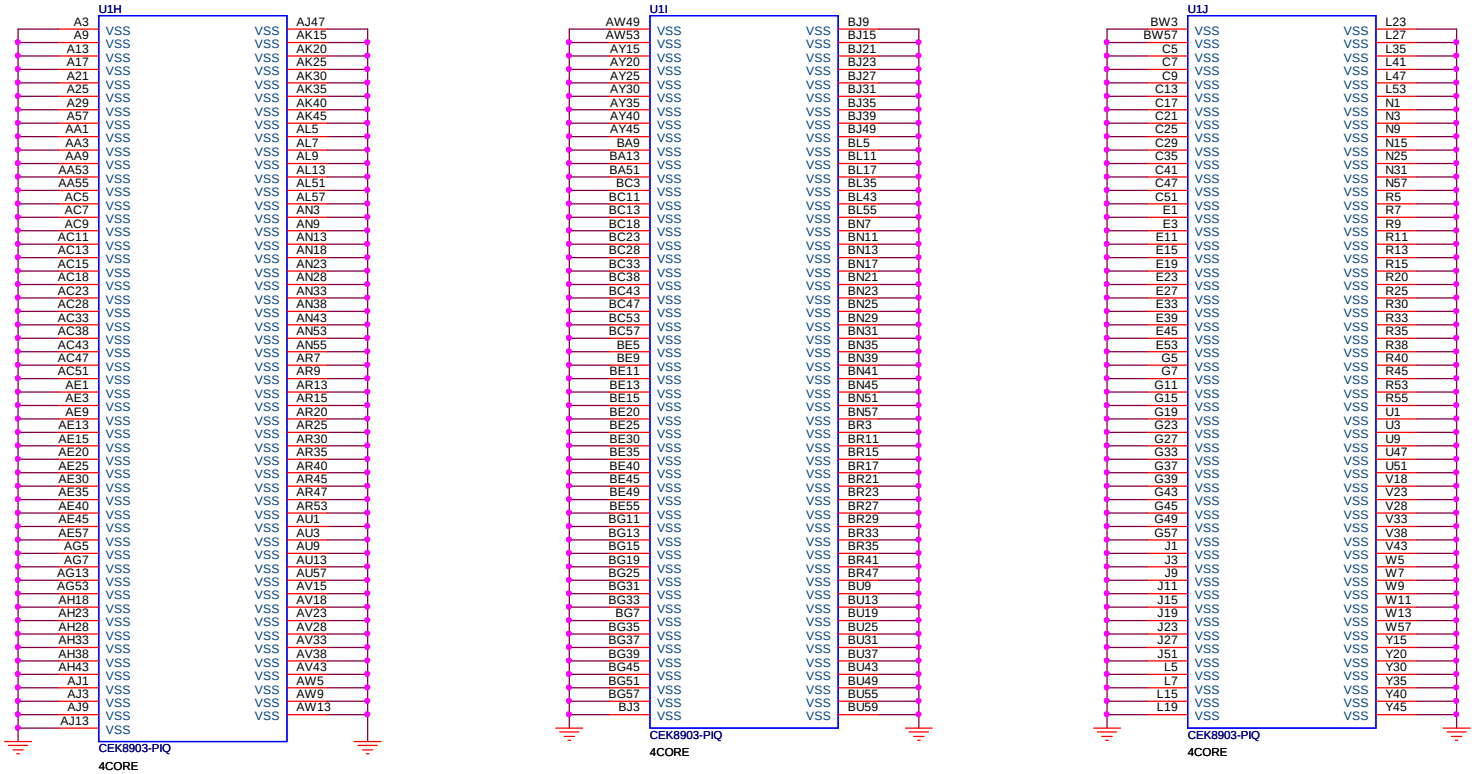

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Title: CPU_VSS

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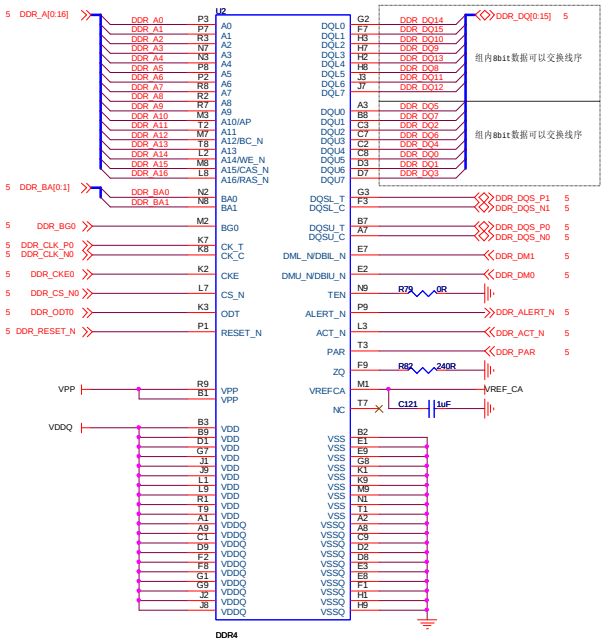
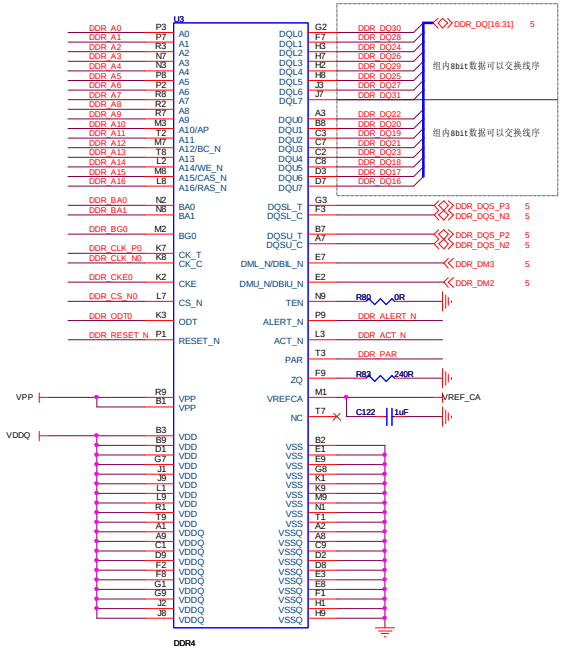
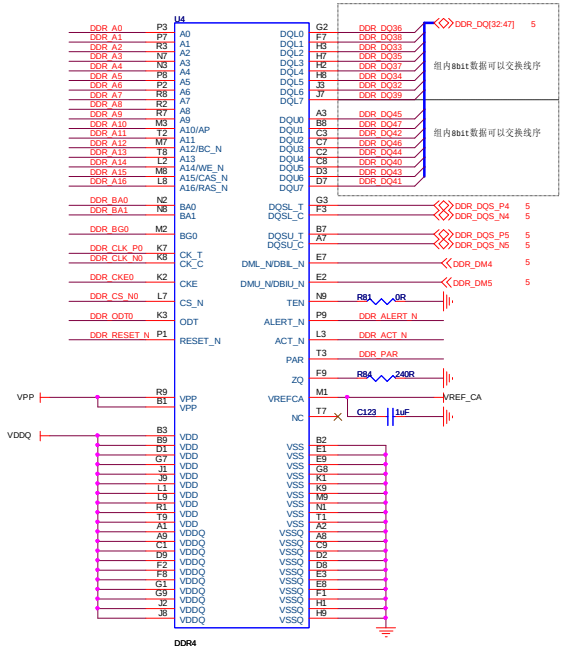
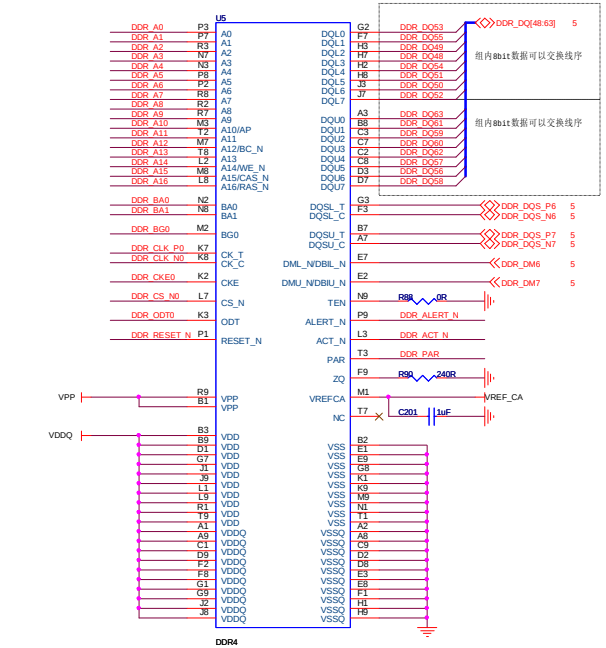
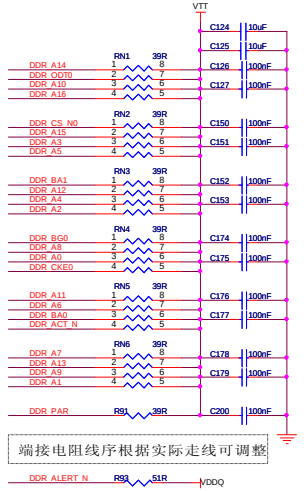


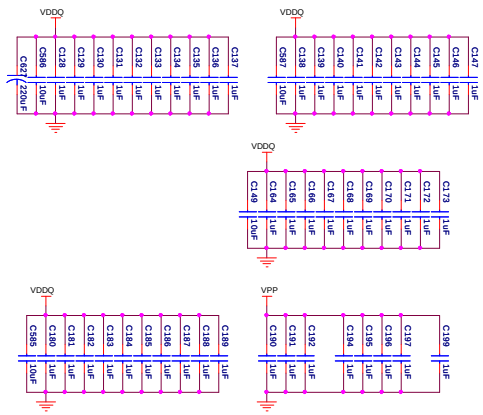


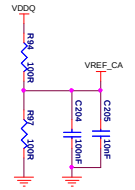


除ECC外，每个slice之间可以交换

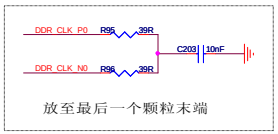








对应手册，C203电容由22nF修改为10nF



放至最后一个颗粒末端

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Title: DDR4_ONBOARD

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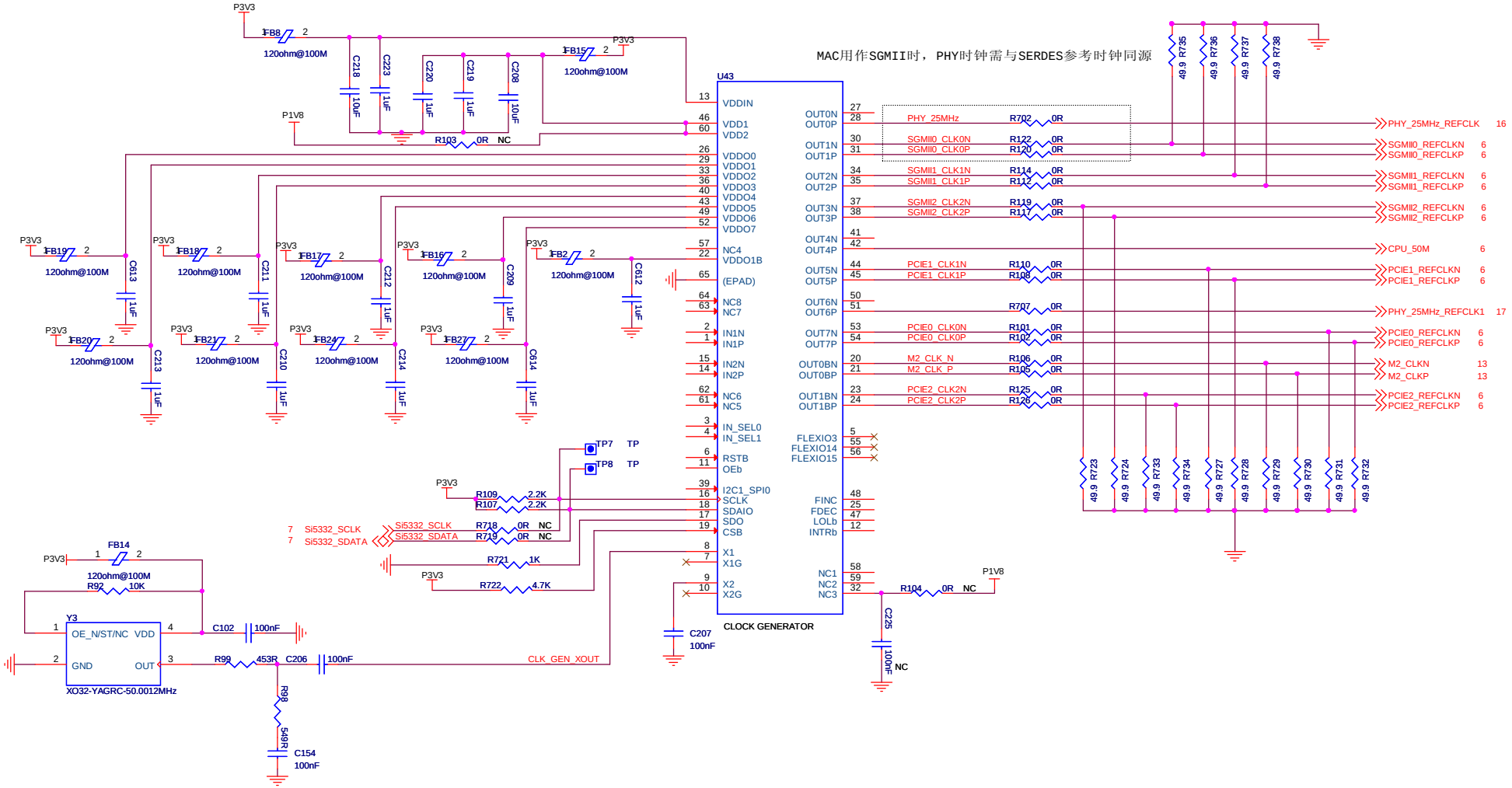

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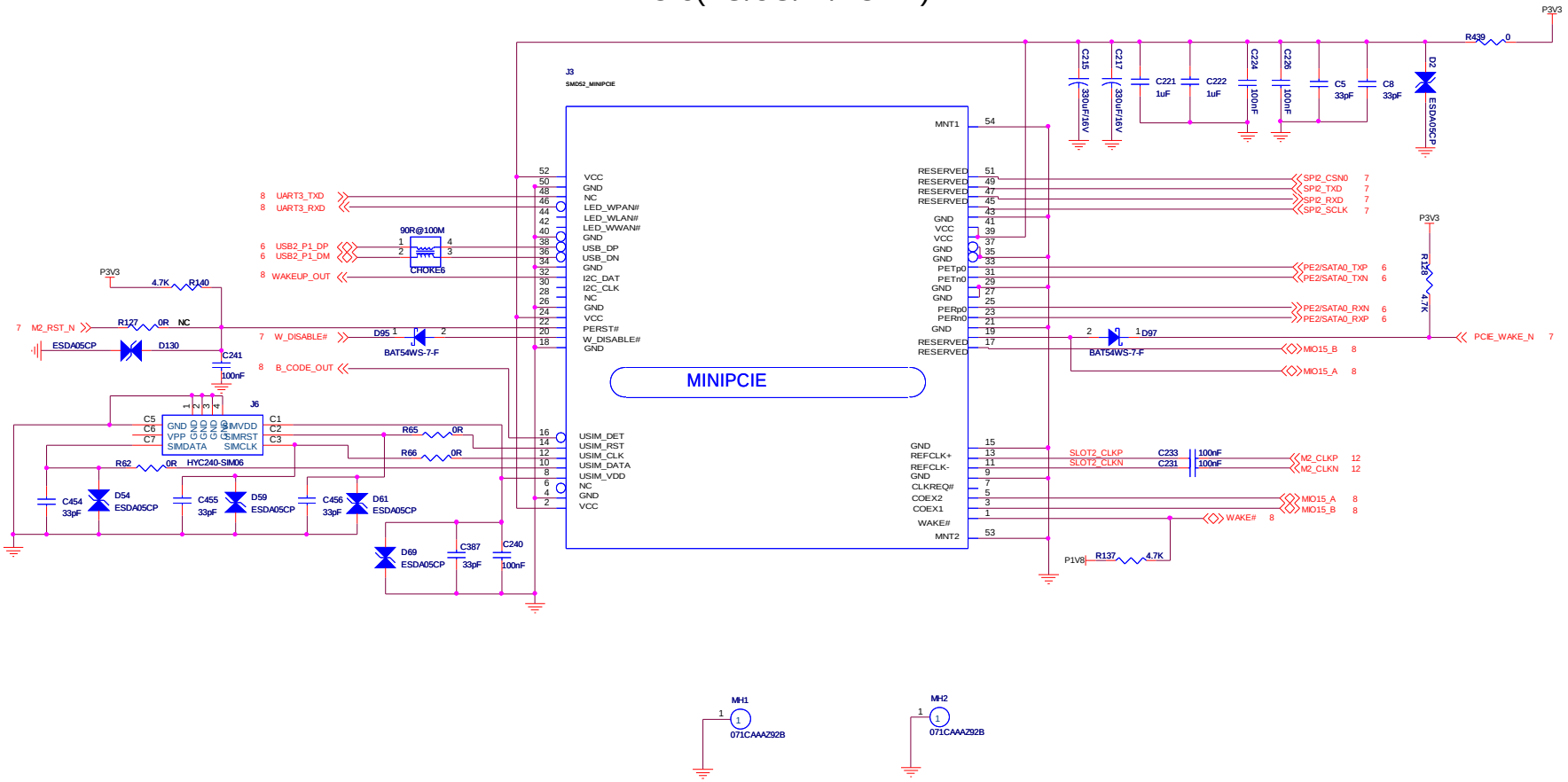
MiniPCIe(4G/5G/AI/LORA)



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Title	MiniPCIe	
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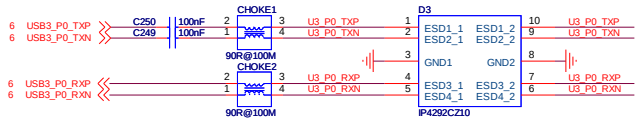
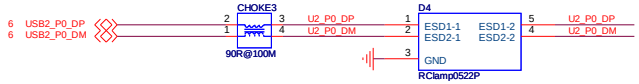
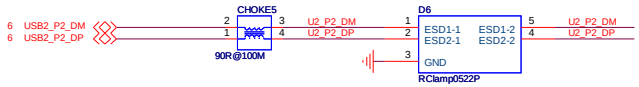
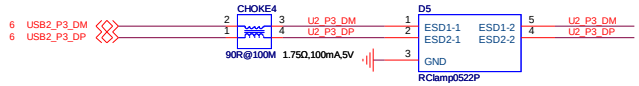
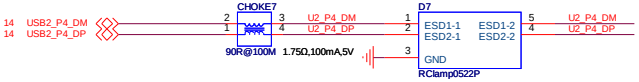
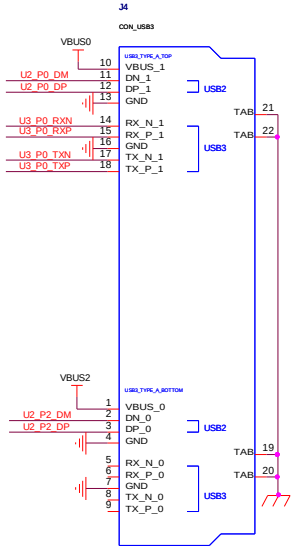


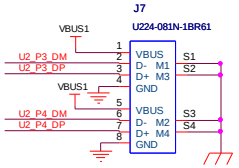




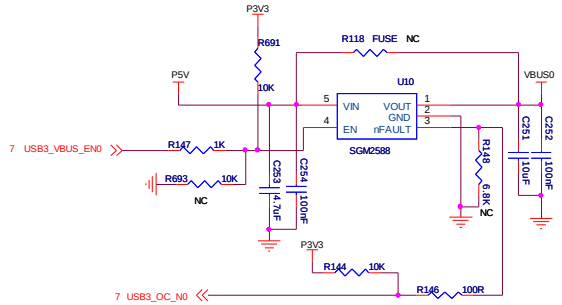




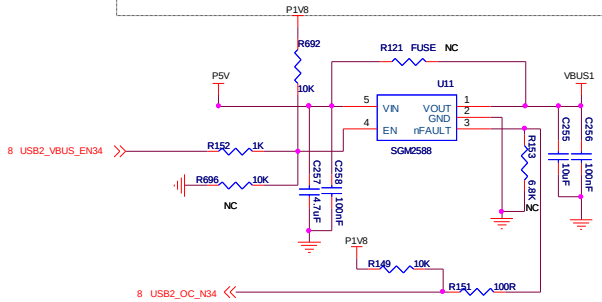




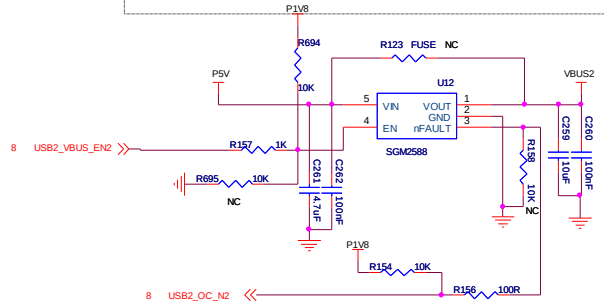
USB3.0和USB2.0做HOST时，VBUS_EN和OC_N可用GPIO代替
用户如需上电直接使能USB，则上拉使能即可（本设计预留）



用户如需上电直接使能USB，则上拉使能即可（本设计预留）



用户如需上电直接使能USB，则上拉使能即可（本设计预留）



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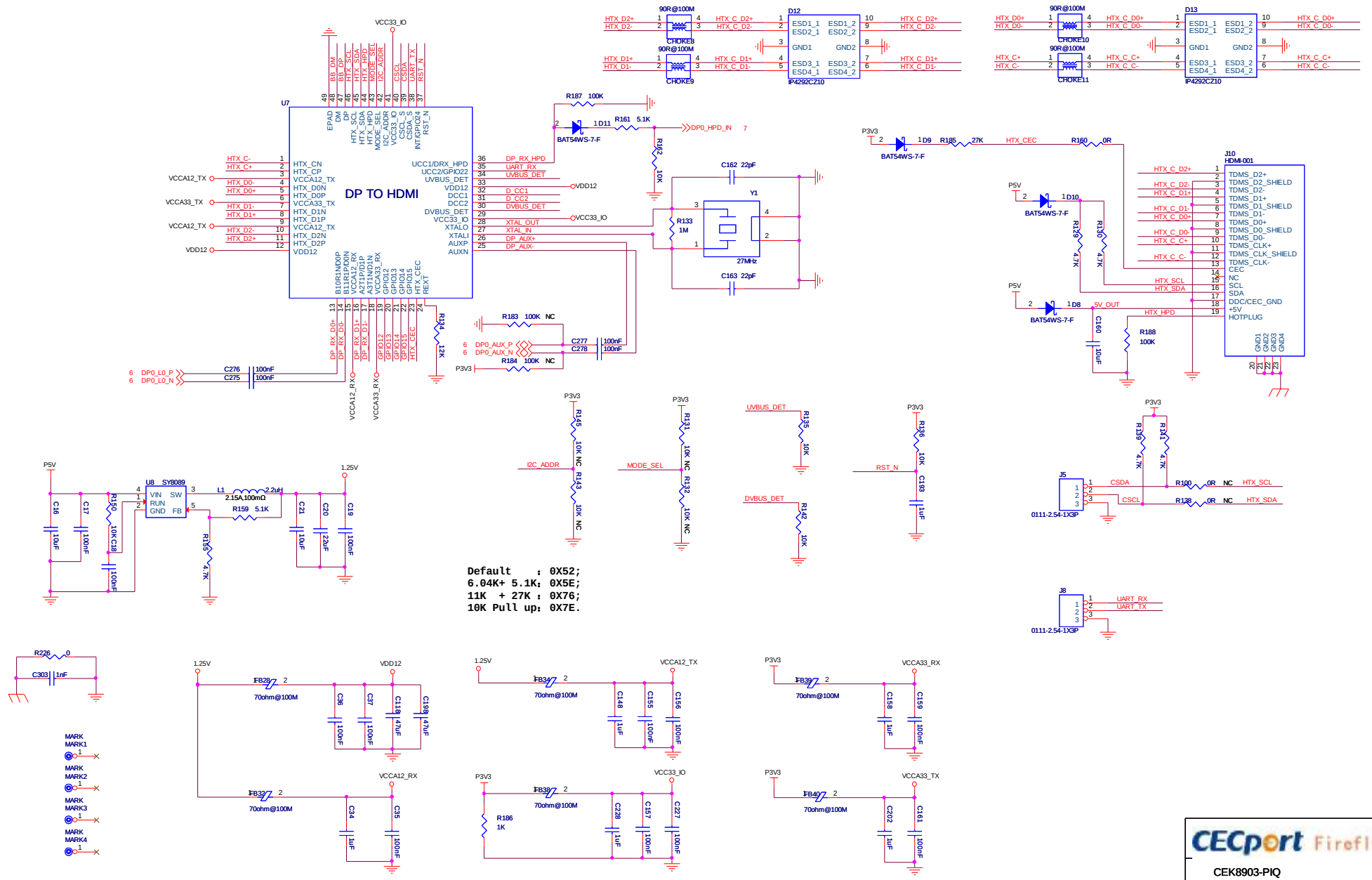
DP TO HDMI
U7
U8 SY8089
J10 HDMI-001
J5
J8
D12
D13
Default : 0X52;
6.04K+ 5.1K: 0X5E;
11K + 27K : 0X76;
10K Pull up: 0X7E.
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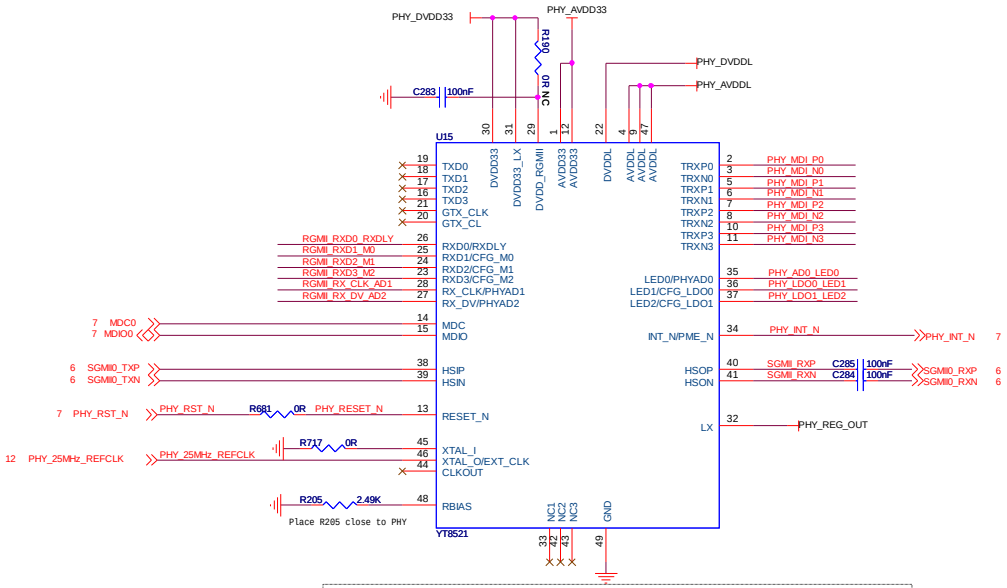
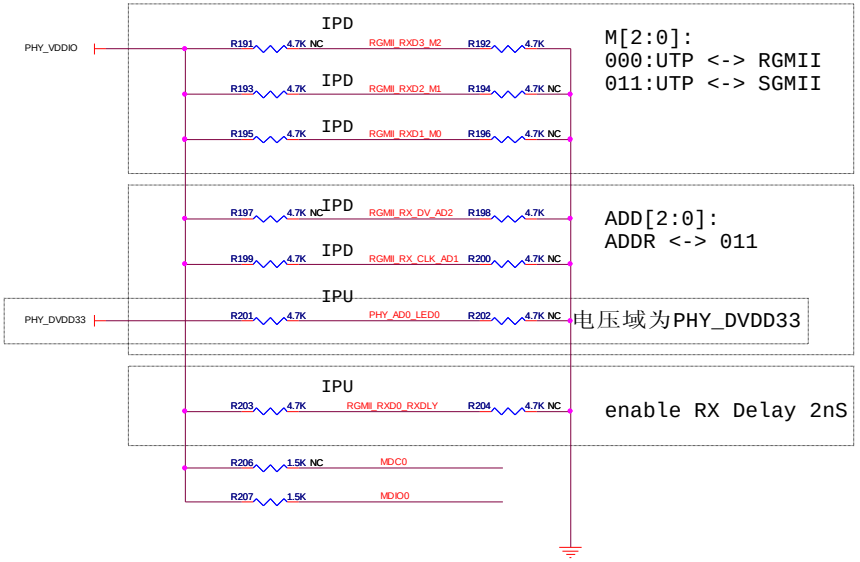
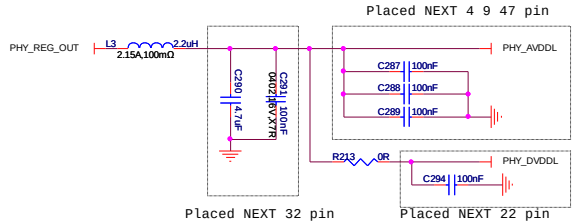
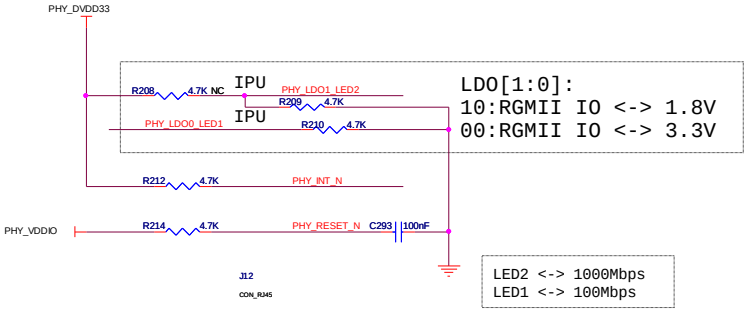
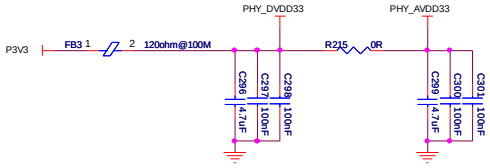


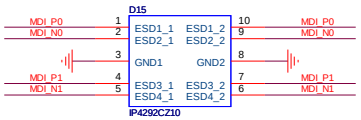
用户可根据实际需求MAC端选择RGMII或者SGMII
本设计使用SGMII



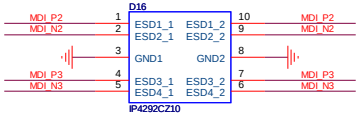




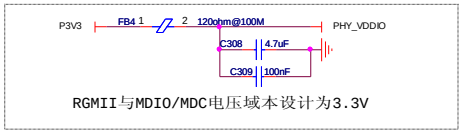




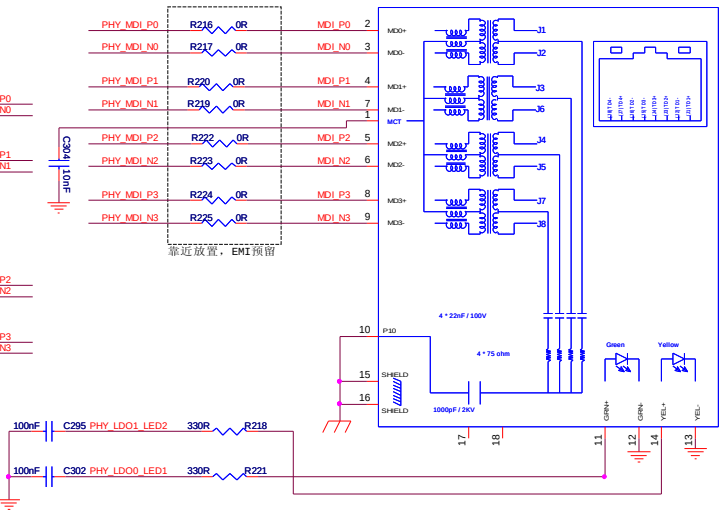
ESD靠近RJ45放置



ESD靠近RJ45放置



RGMII与MDIO/MDC电压域本设计为3.3V



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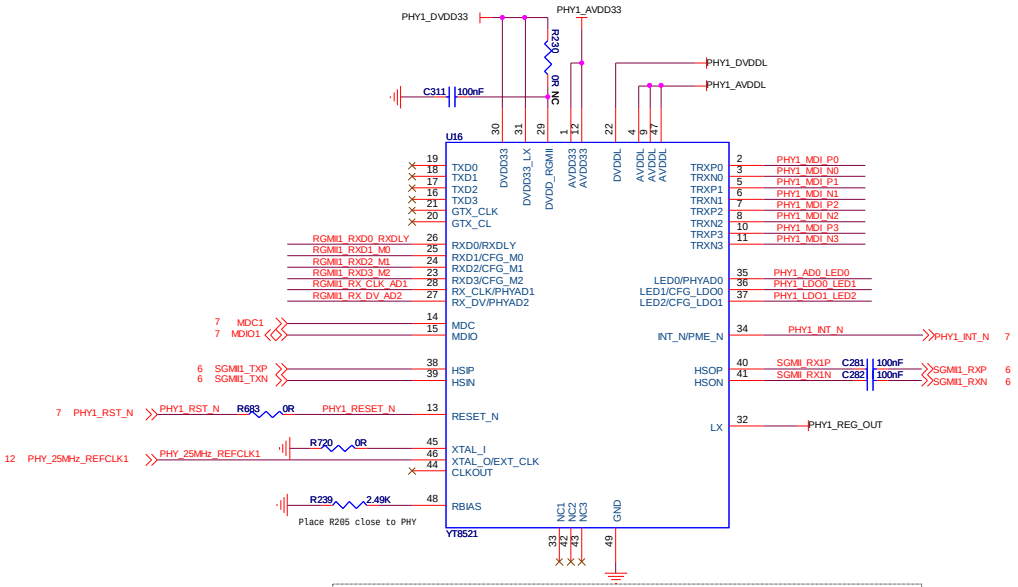
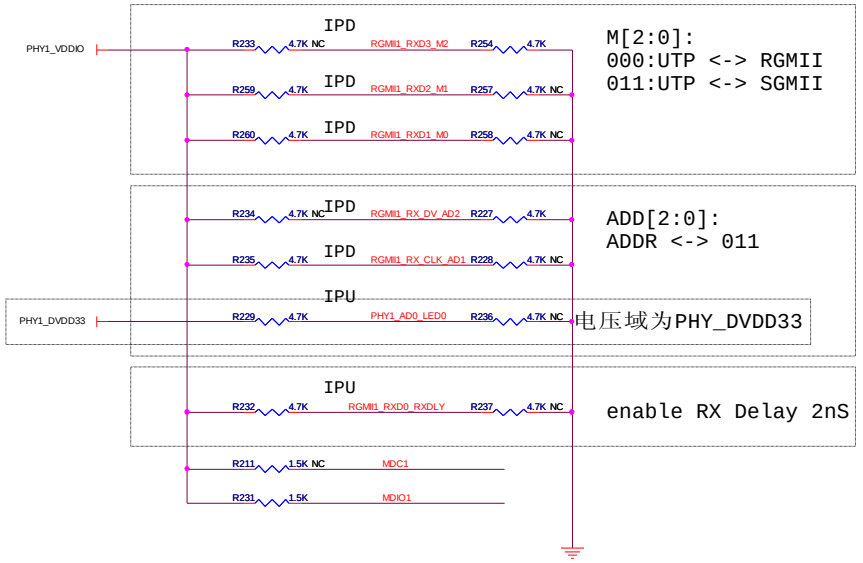
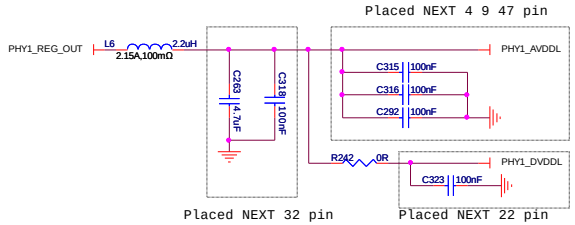
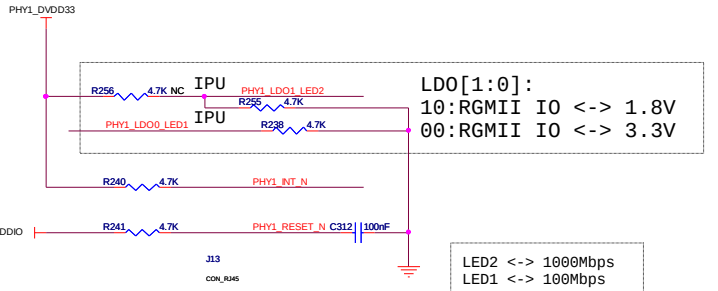
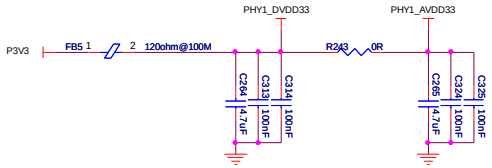


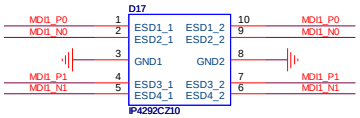


用户可根据实际需求MAC端选择RGMII或者SGMII
本设计使用SGMII

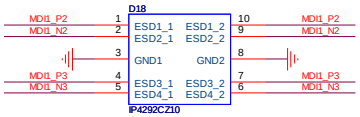


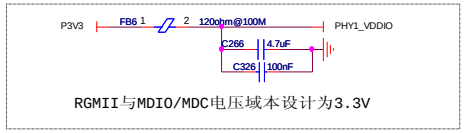


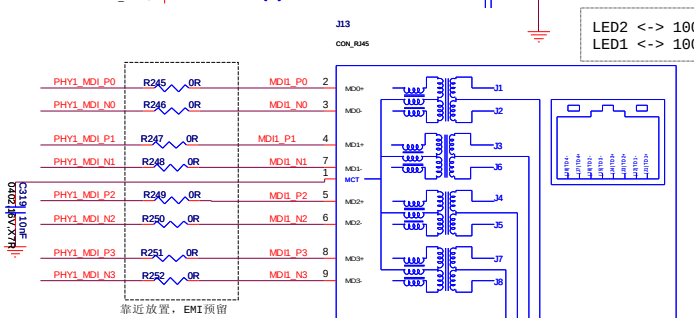




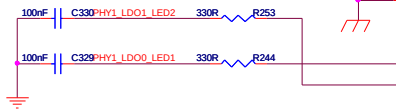
ESD靠近RJ45放置







LED2 <-> 1000Mbps
LED1 <-> 100Mbps



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Title: SGMII1_ETHERNET

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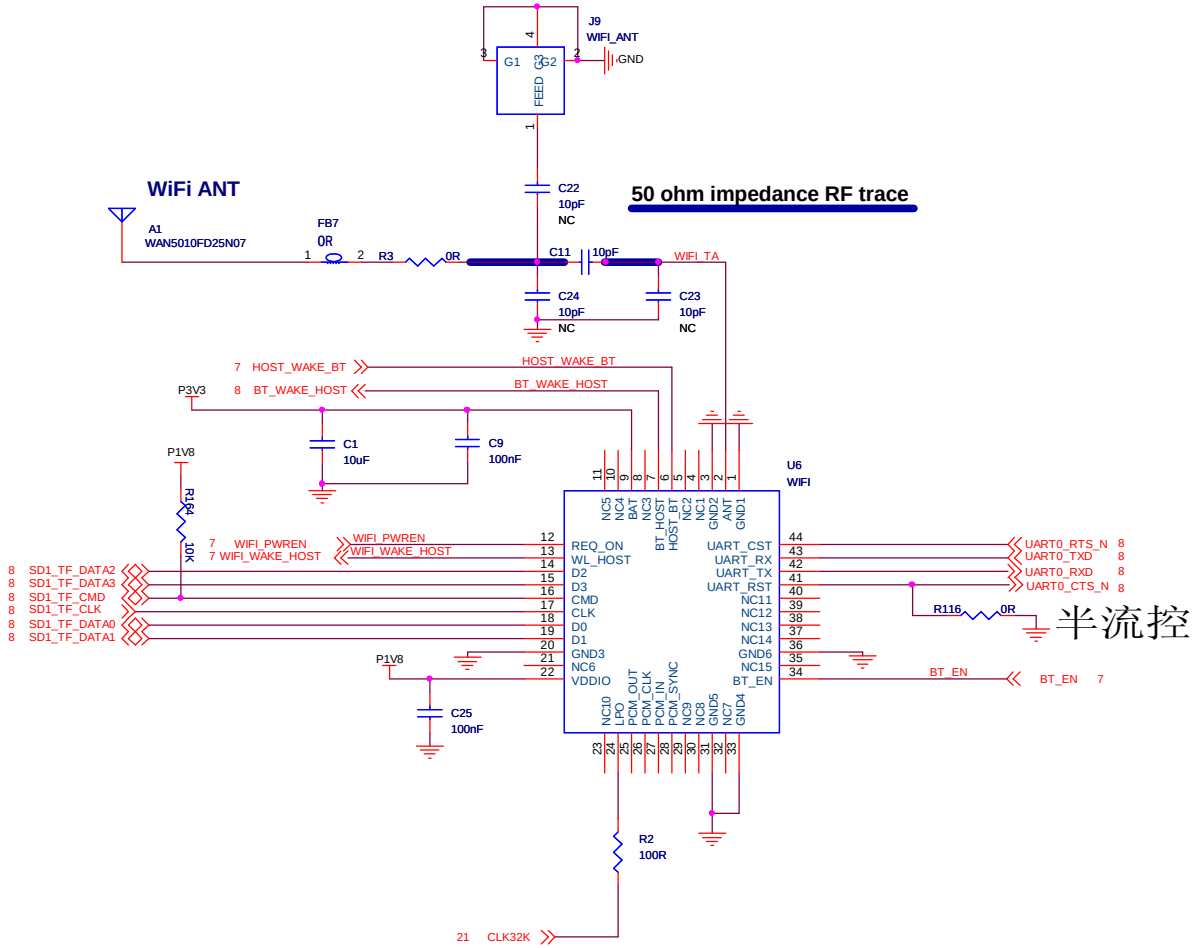

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Title: WIFI&BT

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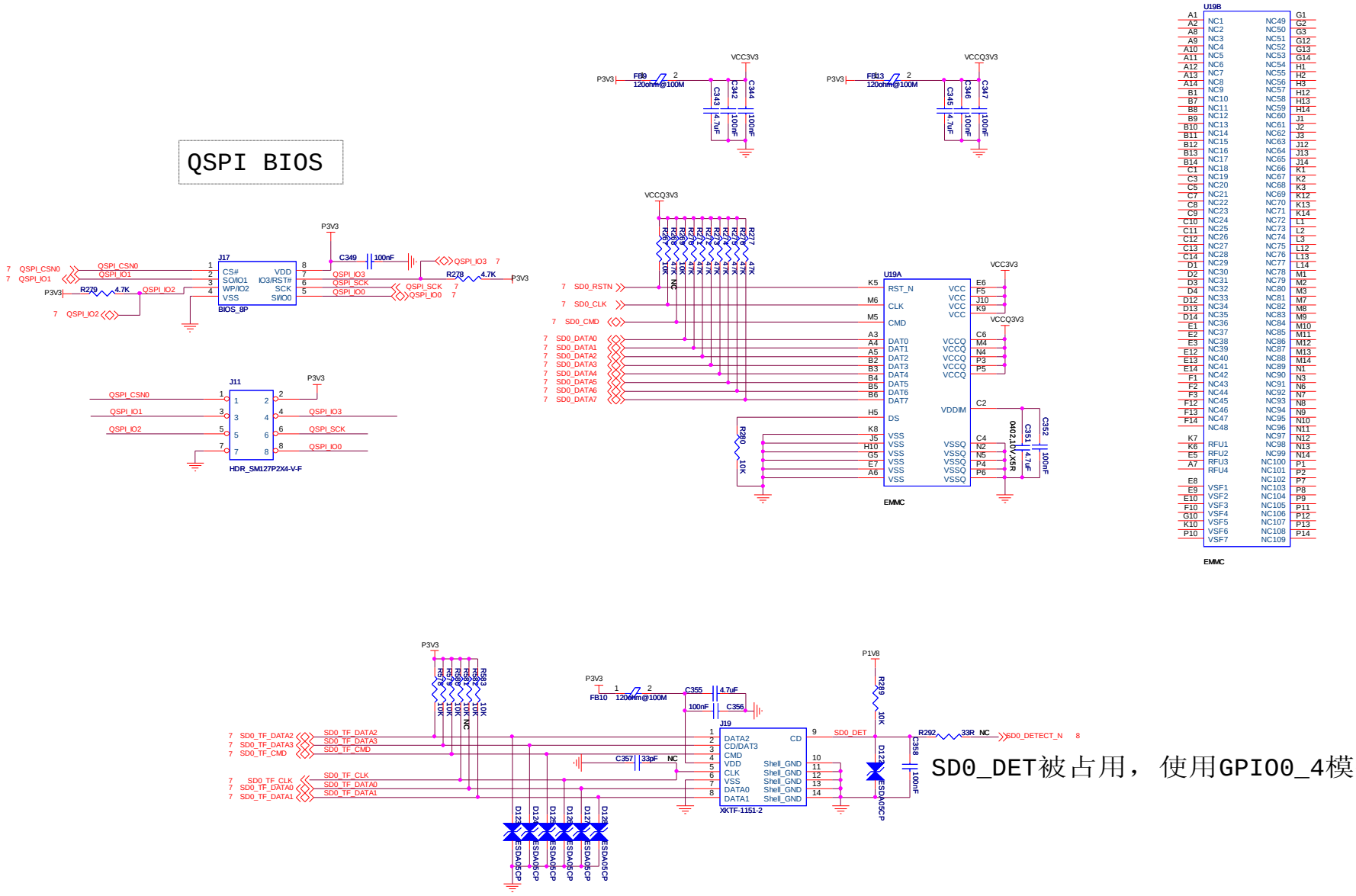
QSPI BIOS
J17
BIOS_8P
J11
HDR_SM127P2X4-V-F
U19A
EMMC
U19B
EMMC
J19
XKTF-1151-2
SD0_DET被占用，使用GPIO0_4模拟
ESD靠近TF卡槽放置
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SD
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Custom
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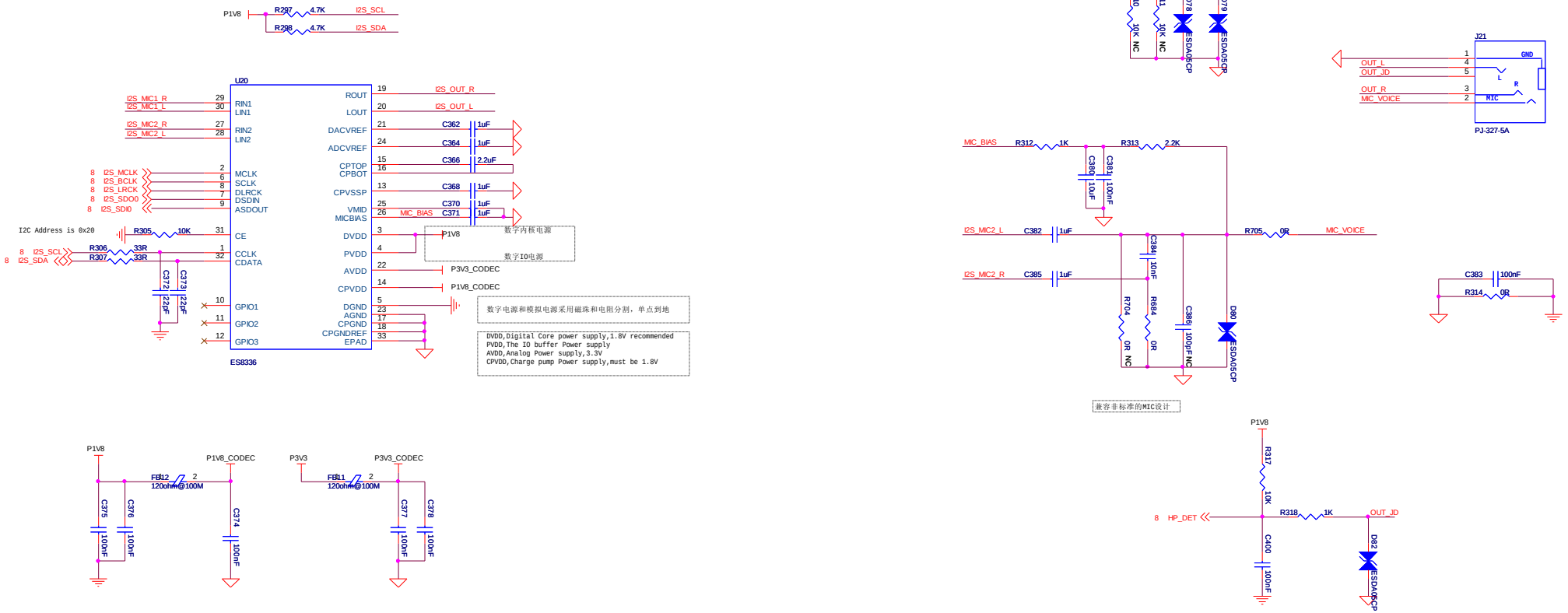

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Title: AUDIO_CODEC

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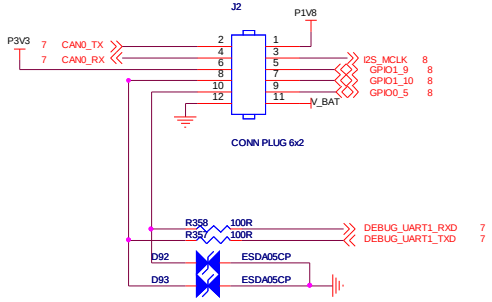
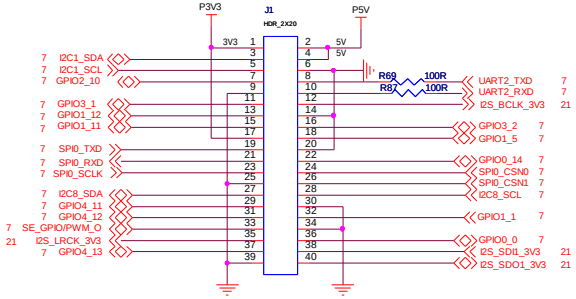
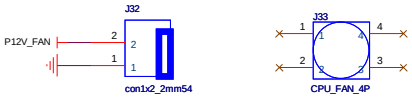
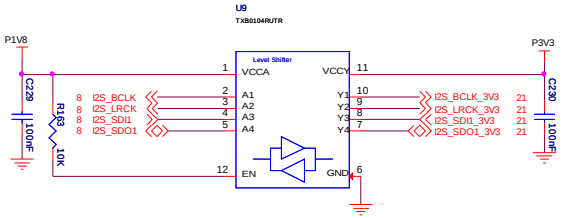
1.8V IO:I2S_MCLK,GPIO0_ 5 ,GPIO1_ 9 10

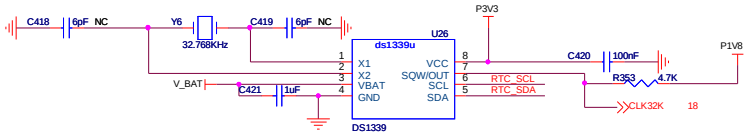


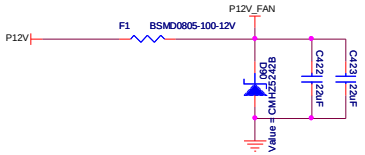
DEBUG UART











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Title: CONN_MISC

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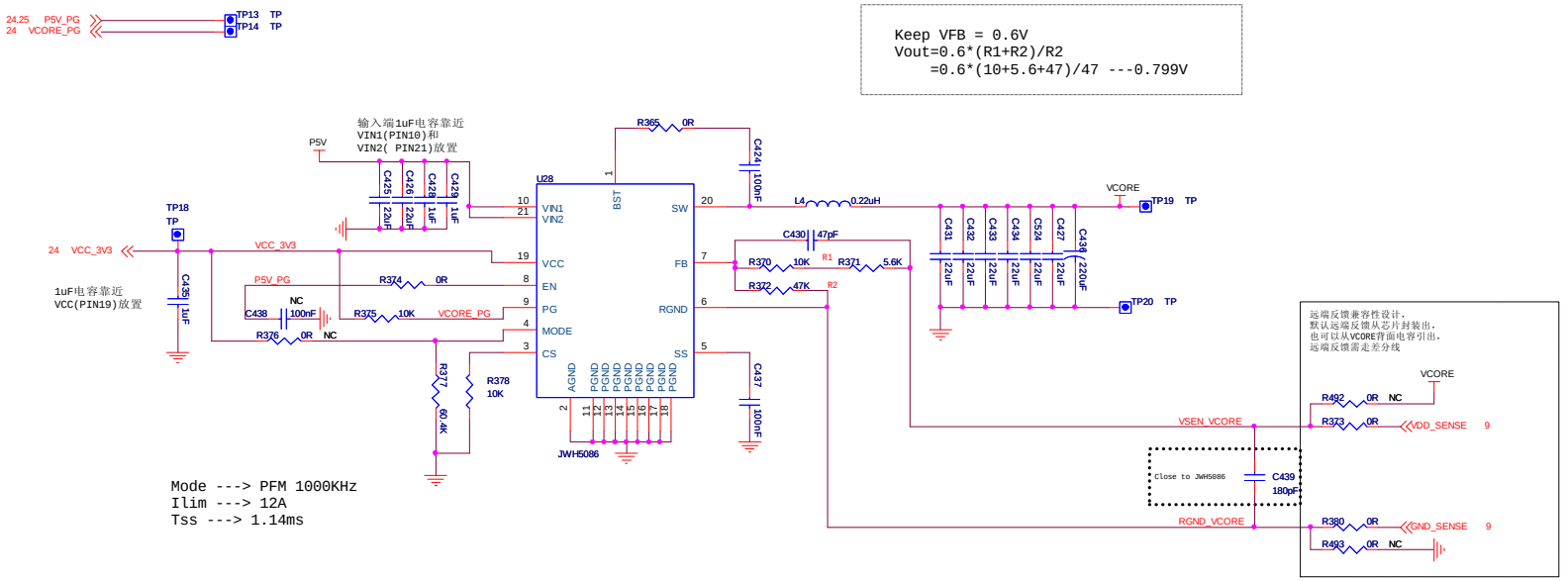

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Title: PWR_VCORE

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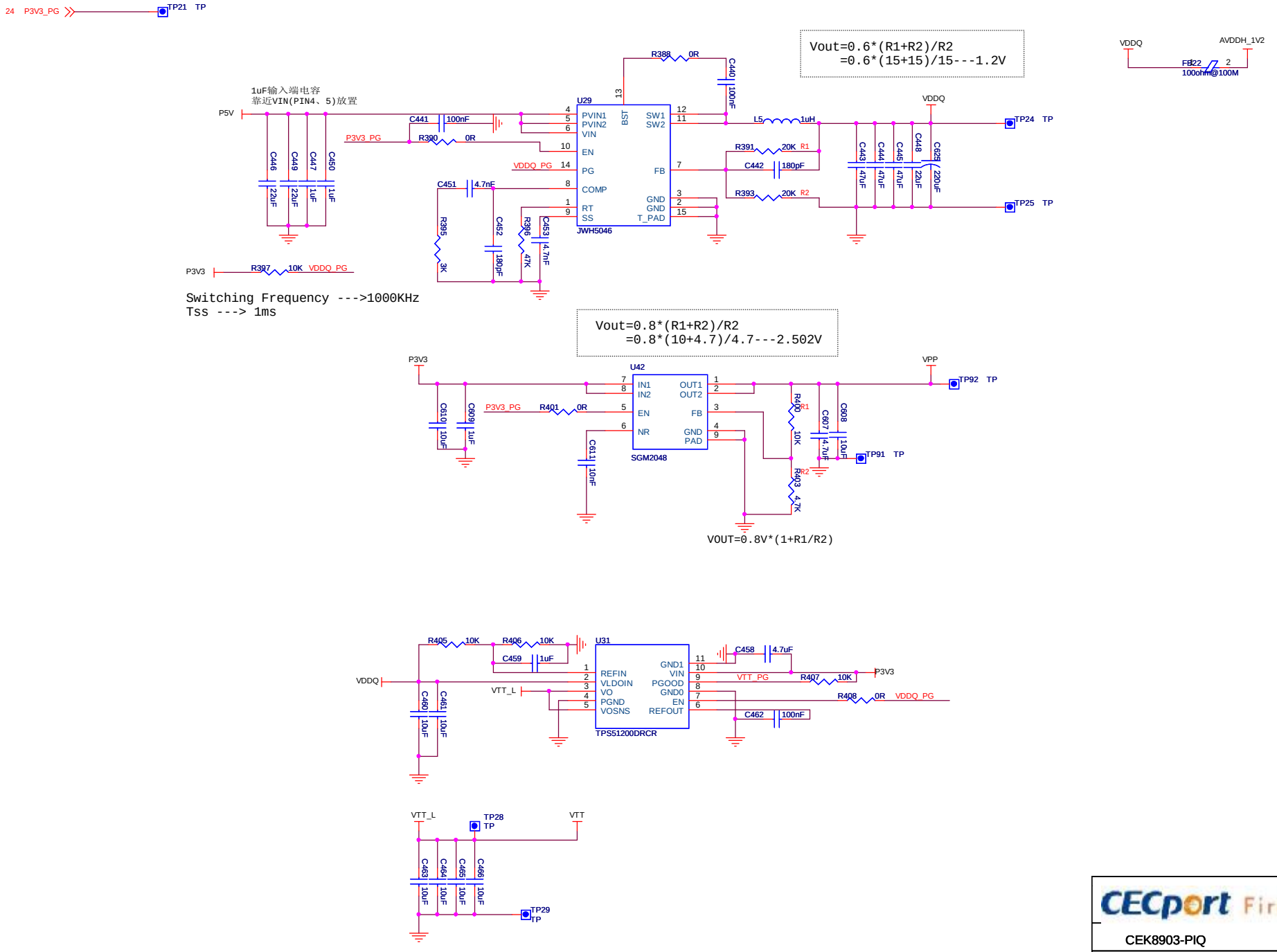

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Title: PWR_VDD&VPP&VTT

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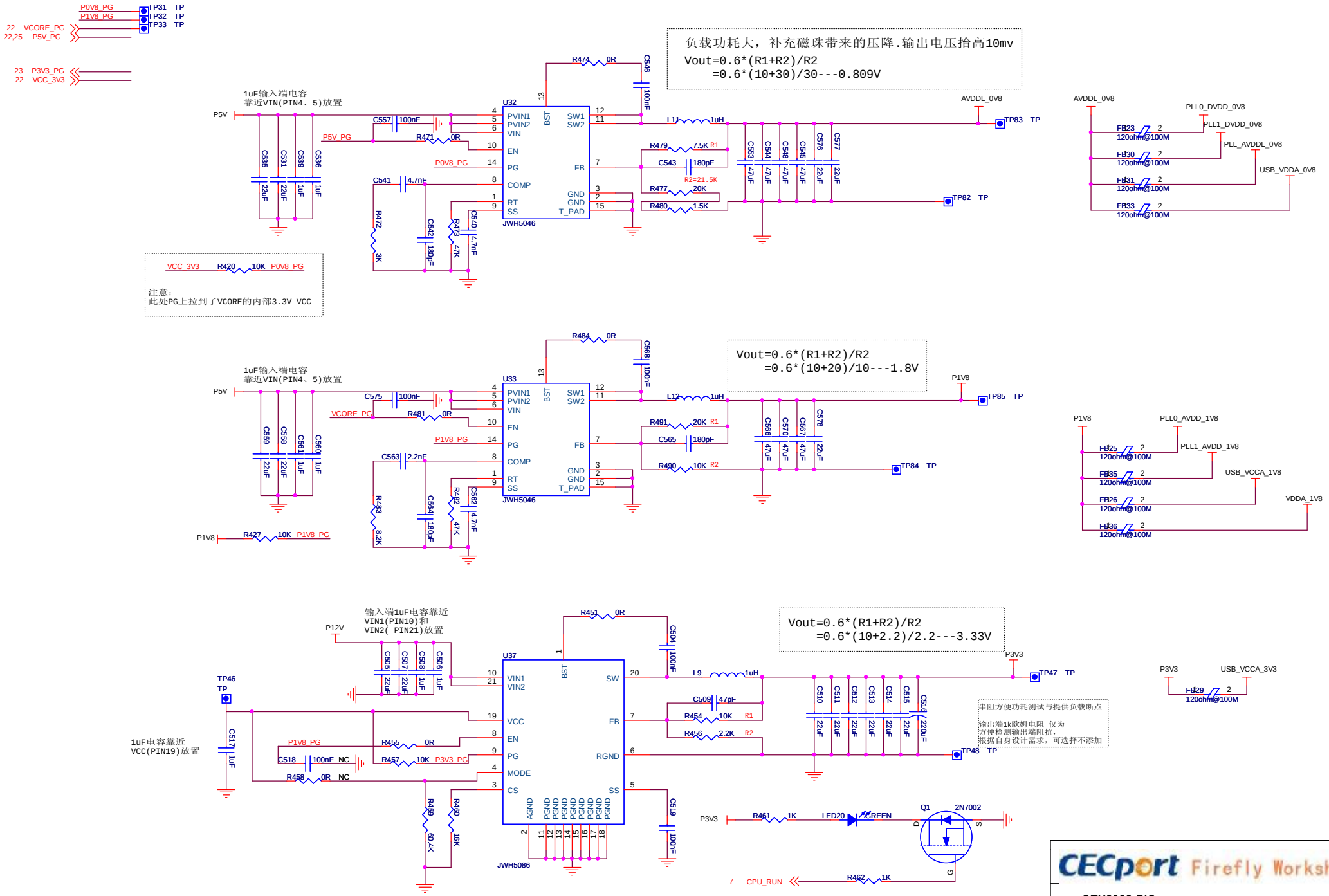

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Title: PWR_P0V8&P1V8&P3V3

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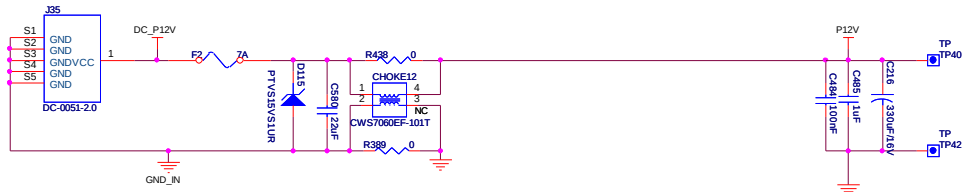
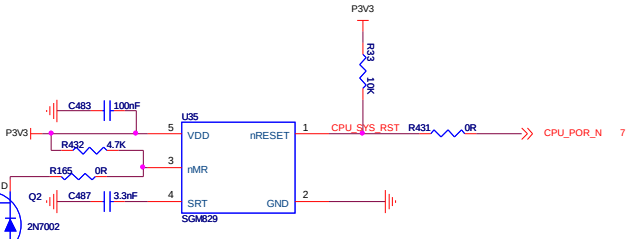
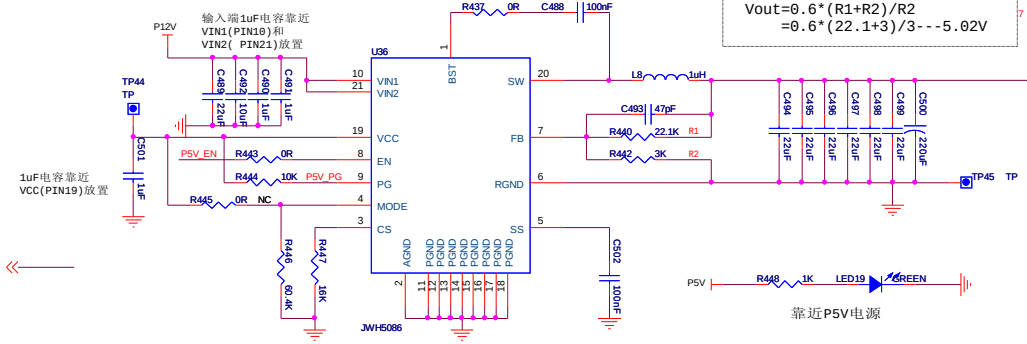




P3V3上电后，延时9.53ms，CPU_SYS_RST再被拉高。

$T_D(us) = (2.8 \times 10^6) \times C_{SRT}(uF) + 290us$



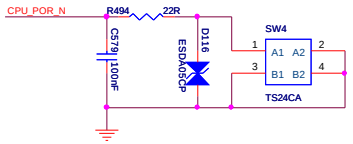
Mode ---> PFM 1000KHz
Ilim ---> 9.5A
Tss ---> 1.14ms

本参考设计有复位按钮、上电复位、FPGA复位三种方式接入了CPU的POR_RST：

1.客户如需使用FPGA做LBC锁存或其它用途，建议使用FPGA控制上电复位，本设计有预留；

2.无FPGA场景，用户可以选择电源PG信号控制上电时序，使用复位芯片上电复位；

3.本设计与参考板对应，为满足电源PG信号控制上电时序示例的同时，验证LBC启动功能，使用FPGA复位CPU（FPGA锁存需要优先CPU复位）。



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Title: PWR_P5V&P12V

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